Development of A 4 x 14-Gbps/ch VCSEL Array Driver ASIC in 65nm CMOS Technology for Detector Front-end Readout in Particle Physics

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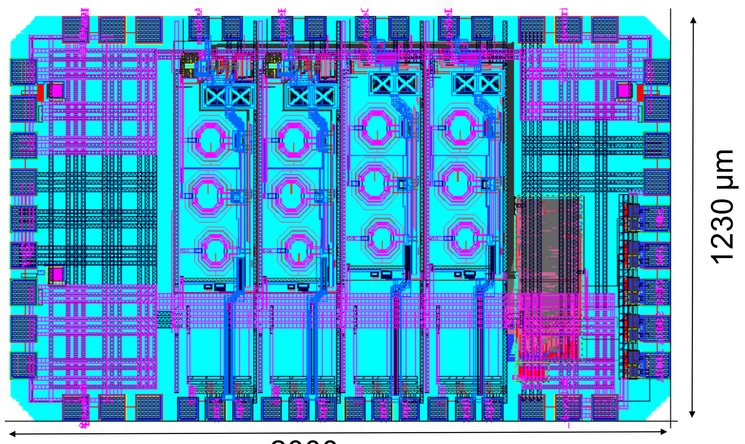
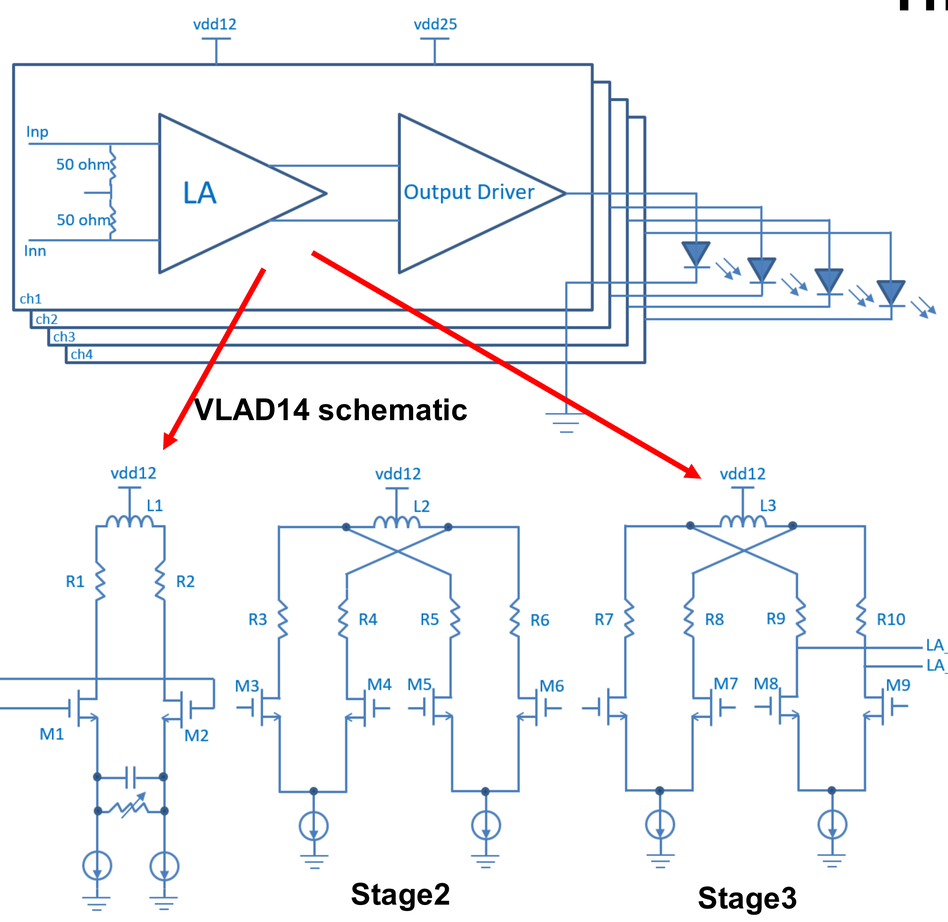


4 x 14- Gbps/ch VCSEL Array Driver (VLAD14)

Introduction

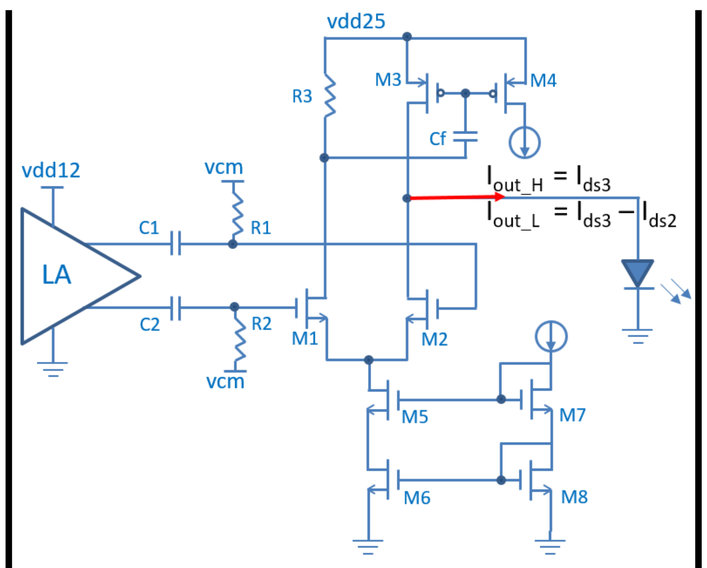
- VLAD14 is a 4-channel, 4 x 14-Gbps VCSEL array driver ASIC, fabricated with a commercial 65nm CMOS technology, aimed for the applications such as detector front-end readout in particle physics and related fields.
- Four channels of VLAD14 have two different designs. They feature power consumptions of 52 mW/ch (Design 1) and 44 mW/ch (Design 2) respectively when delivering a 2 mA ~7 mA output current to the VCSEL. Both designs need 1.2V and 2.5V power supply.
- VLAD14 die measures 2000 µm x 1230 µm
- VLAD14 die was wire bonded to the VCSEL array, integrated within the array optical module and fully tested.

The design of VLAD14



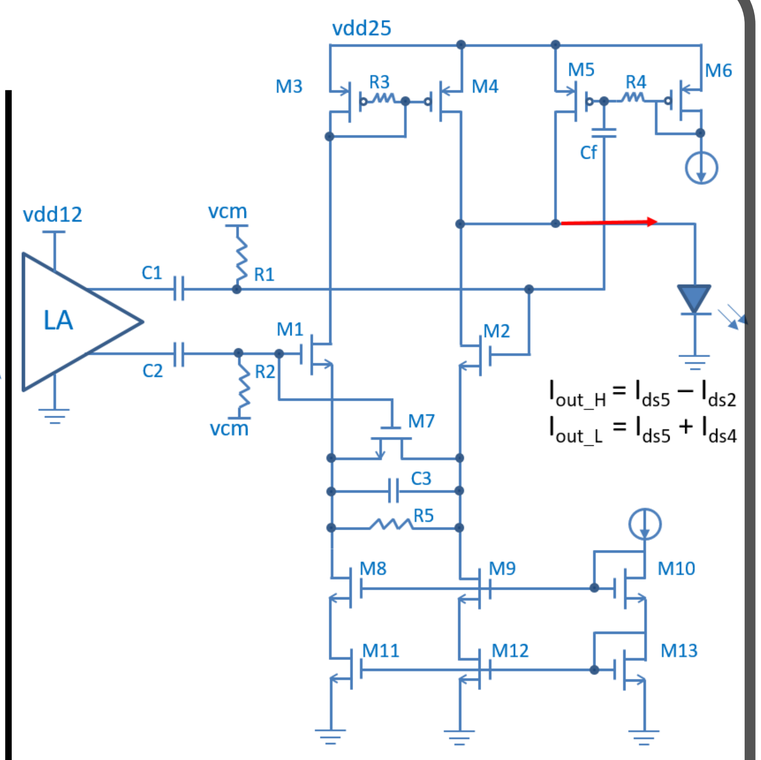
Limiting Amplifier (LA)

- Each channel in VLAD14 consists of a limiting Amplifier (LA) and an output driver. Two designs share the same LA design but adopts different output drivers.
- Limiting amplifier (LA) is composed of three differential stages. Stage1 uses CTLE as the adjustable equalization, and a passive inductance is included to optimize the peaking frequency. Stage2 and Stage3 both employ shared inductance structure, as shown in the picture.



Output Driver Design1

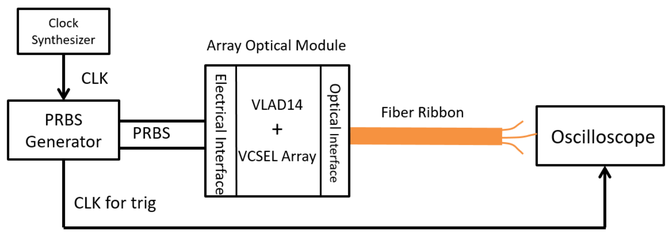
- The principle of this output driver is to divert the current from a PMOS current source (M3) using a current switch (M2) controlled by the LA outputs.
- The output current $\mathbf{I_{out} = I_{ds3} - I_{ds2}}$
- The output stage is AC coupled to the LA to allow independent control of the DC point. M5 and M6 are stacked current source to also increase the DC point of M1, M2 source. Thus, M2 drain can be directly used as the output node to be connected with the VCSEL anode, which has a DC voltage of around 1.8V.

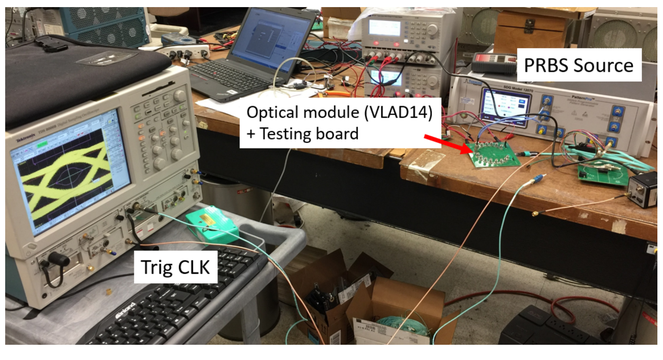


Output Driver Design2

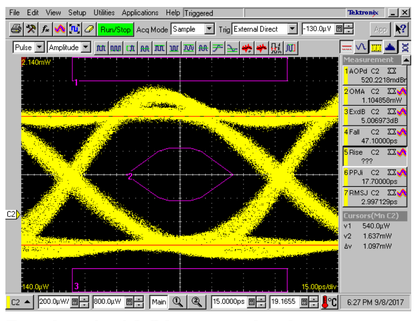
- The PMOS current source (M5) acts as the average current in this output driver design.
- The output current $\mathbf{I_{out} = I_{ds5} + I_{ds4} - I_{ds2}}$. And I_{ds4} and I_{ds2} are complementarily provided. I_{ds4} is mirrored from I_{ds1} by M3, so that the current of the left brunch (I_{ds1}) also contributes to the final output comparing to Design1, making it a more efficient structure.
- The same AC coupling strategy is also used in Design2, and CTLE(C3 and R5) structure is used to improve the bandwidth.

Integration with array optical modules and test results

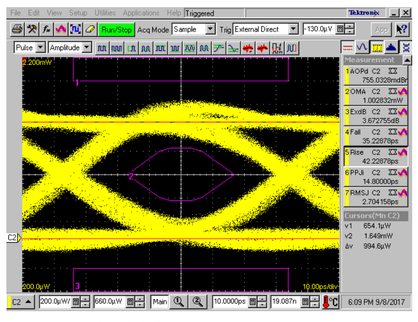




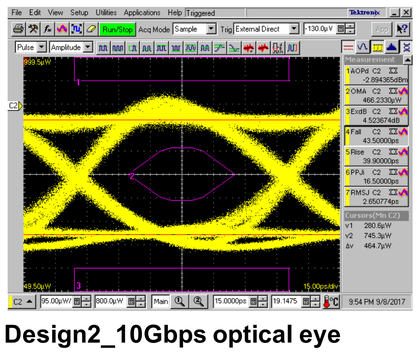
VLAD14 optical eye diagram testing set up



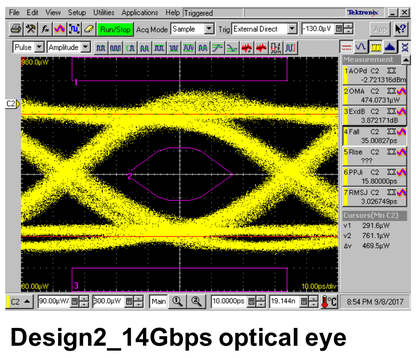
Design1_10Gbps optical eye



Design1_14Gbps optical eye



Design2_10Gbps optical eye



Design2_14Gbps optical eye

- VLAD14 is integrated in an array optical module and tested optically.
- VCSEL Array used in the test: II-VI 14G series: APA4401040201 II-VI
- 10-Gbps/ch and 14-Gbps/ch optical eye diagrams of two designs were captured and shown in the left.
- The eye mask shown in all four pictures is 10GFC (10Gbps Fiber Channel) eye mask.

Conclusion

- A 4-channel, 4 x 14-Gbps VCSEL array driver (VLAD14) is designed with two different output structures and fully tested.
- Both designs show wide-open optical eyes, and pass the eye mask test at the date rate of 14-Gbps/ch.

Acknowledgments

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