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Development of 4 × 28-Gbps and 4 × 14-Gbps VCSEL Array Drivers in 65 nm CMOS for HEP Applications

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We present designs and test results of two radiation-tolerant VCSEL array driver ASICs fabricated in 65 nm CMOS technology, VLAD28 and VLAD14. VLAD28 is a 4 × 28-Gbps driver, delivering 2 mA bias and 5 mA modulation currents with a power consumption of 90 mW/ch. VLAD14 is a low-power 4 × 14-Gbps driver, delivering 2 mA and 6 mA modulation with a power consumption of 44 mW/ch. The two drivers have respective innovative structures in the output stage for high-speed and low-power operation. Full-channel optical tests will be carried out in the summer and the results will be reported at the workshop.

Summary

VCSEL-based, high-speed, low-power, radiation-tolerant short-range optical data links are in high demand for detector data transmission in the LHC upgrades as well as in other physics detector developments. VCSEL array driver ASICs are the key components in the optical links. Last year we presented two designs of 10-Gbps/ch VCSEL array drivers in 65 nm CMOS technology. As an evolution of the development, we will report on further research and design in 65 nm CMOS technology: a high-speed 4 × 28-Gbps/ch VCSEL array driver (VLAD28) and a low-power 4 × 14-Gbps/ch VCSEL array driver (VLAD14).

Each channel in both VLAD28 and VLAD14 consists of an equalizer stage (1.2 V), a four-stage pre-driver (1.2 V) and an output driver (1.2 V, 2.5 V). The equalizer stage is an amplifier with a 3-bit configurable RC degeneration to provide appropriate frequency peaking in 28-Gbps/ch and 14-Gbps/ch applications. It compensates the input high-frequency loss in PCB traces and especially due to bonding wires when the data rate goes up to 28-Gbps/ch. The four-stage pre-drivers in the VLAD28 and the VLAD 14 both adopt the shared inductor structure to enable peaking in the four stages by using only two inductors.

The output driver of VLAD28 is based on the last year's design with the bandwidth boosted by a feed-forward capacitor. We propose on-chip AC-coupling between the pre-driver and the output driver to isolate the two power domains, and adopt a stacked tail-current source in the output stage to ensure the safety of the thin oxide MOS transistors in differential pair. Hence, the cascode NMOS, used at the output branch to sustain the output DC voltage of 1.8 V (due to the VCSEL forward voltage), can be removed to improve the bandwidth effectively by reducing the output capacitance and eliminating the cut-off recovery of the MOS. The output driver of VLAD14 is a new design. It features a novel PMOS current mirror as the load of the differential MOS without bandwidth degradation, so that the current at the output branch could be –Imod ˜ Imod, instead of the 0 ˜ Imod in the regular design. The modulation efficiency is improved from the structure level in VLAD14.

Both VLAD28 die and VLAD14 die have a size of 2000 µm × 1230 µm. They receive 200 mVp-p differential CML signals as inputs. In the default settings, VLAD28 outputs a 2 mA bias current and a 5 mA modulation current at 28 Gbps/ch with the power consumption of 90 mW/ch, and VLAD14 outputs a 2 mA bias current and a 6 mA modulation current at 14 Gbps/ch with the power consumption of 44 mW/ch. Both designs have been submitted for fabrication in February, 2017, and are expected to be tested electrically and optically during the summer of 2017. The full-channel optical link tests will be conducted, and the results will be reported in the conference.

Primary authors: Dr GUO, Di (Southern Methodist University (US)); Dr SUN, Quan (Department of Physics, Southern Methodist University, Dallas, TX 75275, USA); Dr GONG, Datao (Department of Physics, Southern Methodist University, Dallas, TX 75275, USA); Mr ZHOU, Wei (Department of Physics, Central China Normal University, Wuhan, Hubei 430079, P.R. China); GAO, chaosong (Central China Normal University); LIU, Chonghan (Southern Methodist University); LIU, Tiankuan (Southern Methodist University (US)); WANG, Jian (Univ. of Sci. & Tech. of China); XIANG, annie (Southern Methodist University); Dr XIAO, Le (Department of Physics, Central China Normal University, Wuhan, Hubei 430079, P.R. China); Mr YANG, Dongxu (Department of Physics, Southern Methodist University, Dallas, TX 75275, USA); YE, Jingbo (Southern Methodist University (US))

Presenter: Dr GUO, Di (Southern Methodist University (US))

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