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CACTµS : High-Voltage CMOS Monolithic Active Pixel Sensor for Tracking and Time Tagging of Charged Particles

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The increase of luminosity foreseen for the Phase-II HL-LHC upgrades calls for new solutions to fight against the expected pile-up effects. One approach is to measure very accurately the time of arrival of the particles with a resolution of few tens of picoseconds. In addition, a spatial granularity better than a few millimeter will be needed to obtain a fake jet rejection rate acceptable for physics analyses. These goals could be achieved by using the intrinsic benefits of a standard High-Voltage CMOS technology -in conjunction with a high-resistivity detector material- leading to a fast, integrated, rad-hard pixel sensor ASIC.

Summary

The increase of luminosity foreseen for the Phase-II HL-LHC upgrades will lead to an unprecedented occupancy of the detectors. A solution proposed to fight against the resulting pile-up effect is to measure very accurately the time of arrival of the particles with a resolution of a few tens of picosecond. This allows to reject by the time of flight technique the tracks associated with random pile-up vertices spread longitudinally along the protons bunches collisions. In addition, a spatial granularity better than a few millimeter will be needed to obtain a fake jet rejection rate that is acceptable for the physics analyses. Such performances should be obtained with a sensor also able to cope with the very important radiation levels expected by HL-LHC (up to 6×1015 1 MeV equivalent n/cm2 and 6.5 MGy).

These goals could be reached using the intrinsic benefits of the High-Voltage (HV) CMOS technology. This technology achieves in a standard process a high electric field by isolating the transistor devices -working with standard power supplies- into the collecting diodes. The technology supports high-resistivity (HR) wafers (about 2 kΩ·cm) leading to a complete depletion of the charge sensitive area (> 100 µm depth) of thinned sensors, enhancing the tolerance to neutrons damages.

Proofs of the detection capability and radiation hardness have already been produced for HV-HR technology. We will present here the architecture and simulation results of a 100 mm² pixel sensor, called CACTµS, dedicated to timing measurements. Device (TCAD) simulations and electrical simulations studies based on the HV-HR CMOS LFOUNDRY 150 nm technology design kit have been made to prepare a submission of the Cactus chip. These simulations have shown that a resolution of the order of 50 to 80 ps per MIP impact point can in principle be reached for a HV-CMOS MAPS pixels sensor with 1 mm pixel pitch.

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