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A Full Custom ASIC for Large Area 4-Dimensional Tracking

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Large area silicon trackers with excellent time and position resolution are now considered in the upgrade programs of the ATLAS and CMS detectors.

In this contribution we present the development of a custom ASIC chip meant to be bump-bonded to segmented Ultra-Fast Silicon Detector, aiming to achieve a combined time resolution of $\sigma \sim 30$ ps.

The ASIC is implemented in standard CMOS 110 nm technology.

Summary

The design of large area 4-dimensional silicon tracking detectors with excellent time and position resolutions requires the development of specialized silicon sensors and appropriate electronics.

The silicon sensor that we deemed appropriate for this project are the so called Ultra-Fast Silicon detectors (UFSD). UFSD are a novel type of silicon detectors based on the Low-gain avalanche diode design: the controlled internal gain combined with an appropriate sensor geometry allow having large and short current signals, ideal for timing measurements. Beam test results have demonstrated the capability of UFSD to achieve a time resolution of ˜ 30 ps.

In this contribution we present the first development of a custom built ASIC specifically designed to read-out large area Ultra-Fast Silicon detectors (UFSD) with a time resolution of ˜ 30 ps.

The readout ASIC is implemented in a standard CMOS 110nm technology and organized as a 4x24 pixel matrix, flip-chip assembled to the tentative 1x3 mmˆ2 sensor pads. The on-pixel circuitry includes amplification, timing discriminator and a low power TDC with sub-50 ps binning. The timing discriminator incorporates both constant fraction (CFD) and leading-edge modality. Charge measurement is also provided to allow for off-line calibration of systematic amplitude-related effects. The baseline option for the TDC is to re-use an already existing IP employing time-interleaved analogue interpolators. A topology built with ring oscillators will also be considered.

The pixel logic, working with a clock frequency of 320 MHz or above, manages data building, local configuration, and the operation of the TDCs. This architecture is expected to keep the per-pixel power budget below 5 mW, yielding the necessary 30 ps r.m.s. time resolution. Data, clock, configuration and control signals are propagated asynchronously from pixel to pixel.
The end-of-column logic reads and stores event data from each 24-pixel column, manages the global configuration (periphery bias and chip operation), and serialises the data stream which is then output through 4 640 Mb/s LVDS links.
Preliminary simulation studies based on silicon-proven IP architectures were started, intended to define the rate capability and the readout strategy.
The first reticle-size prototype is expected to be taped-out during 4Q 2018.

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