# A 65nm CMOS Front-End with Zero Dead Time for Next Generation Pixel Detectors


[1] University of Bergamo
Department of Engineering and Applied Sciences
Dalmine (BG), Italy

[2] University of Pavia,
Department of Electrical, Computer and Biomedical Engineering,
Pavia, Italy

[5] Institute of Nuclear Physics (IPNL), CNRS/IN2P3, Lyon, France

L. Gaioni[1,3], D. Braga[4], D. Christian[4], G. Deptuch[4], F. Fahim[4], B. Nodari[5], L. Ratti[2,3], V. Re[1,3] and T. Zimmerman[4]

[3] INFN
Sezione di Pavia
Pavia, Italy

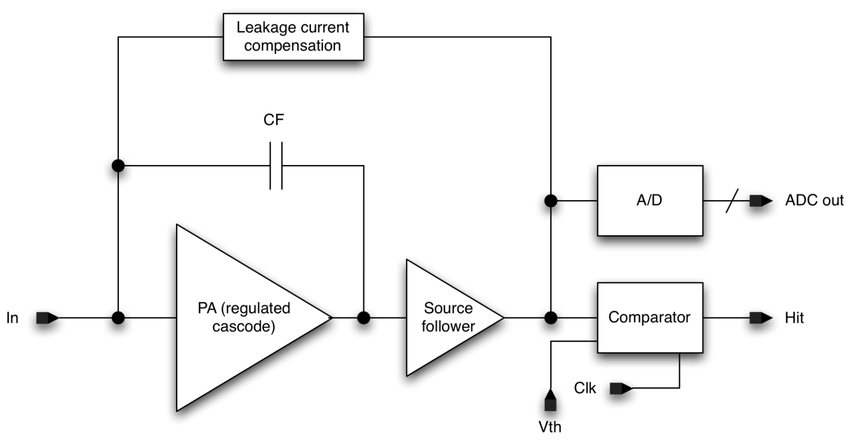
[4] Fermilab
Batavia IL, USA


## Introduction

The next generation of pixel chips at the **High-Luminosity LHC** (HL-LHC) will operate with extremely high particle rates and radiation levels. In the so-called Phase II upgrade, ATLAS and CMS will need a completely new tracker detector, complying with the very demanding operating conditions and the luminosity delivered by the machine (up to 5 x $10^{34}$ $cm^{-2}s^{-1}$ in the next decade). The **65 nm CMOS technology** node exhibits a high degree of radiation tolerance and allows the integration of very dense in-pixel analog and digital functions. It is the target technology of the design community for the development of readout chips for the innermost pixel layers of ATLAS and CMS at the HL-LHC.

In the framework of CERN's **RD53 Collaboration**, a **synchronous analog processor** with **zero dead time** has been designed in a 65 nm CMOS technology. Prototyped in a 16x16 pixel matrix, it includes a low-noise, fast charge-sensitive amplifier featuring a detector leakage compensation circuit and a compact, single-ended comparator with autozeroing capabilities. A 2-bit Flash ADC follows the preamplifier for synchronous conversion.

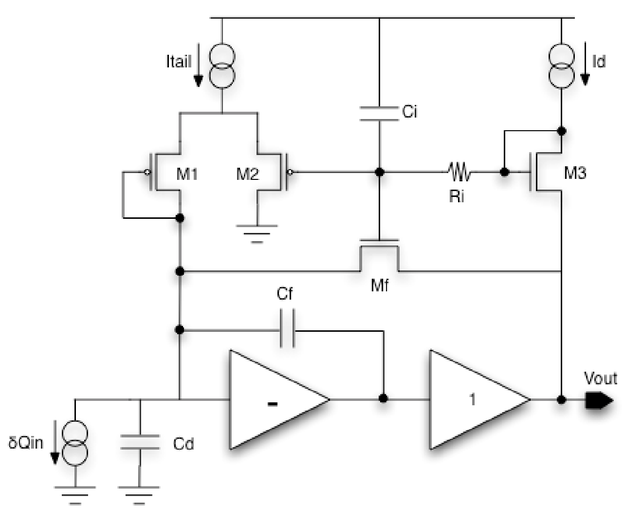
## Analog Front-end



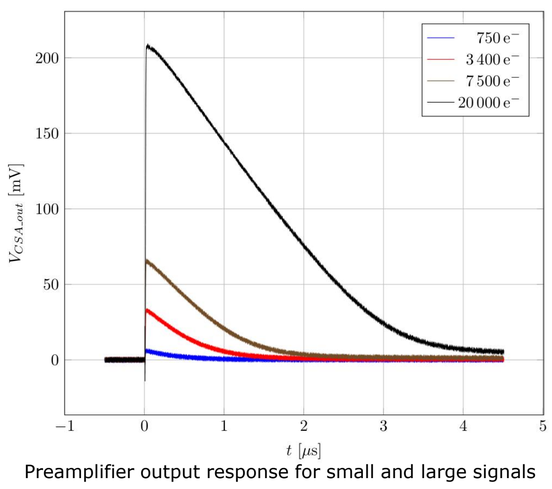

- **Charge sensitive amplifier** based on a regulated cascode gain stage and featuring leakage current compensation
- Compact, single-ended **threshold discriminator** featuring autozeroing, operated with the 40 MHz clock. This implementation is ideally insensitive to device threshold voltage mismatch → trimming DAC not required
- **2-bit Flash ADC** for digital conversion immediately after the preamplifier

## Measurement results

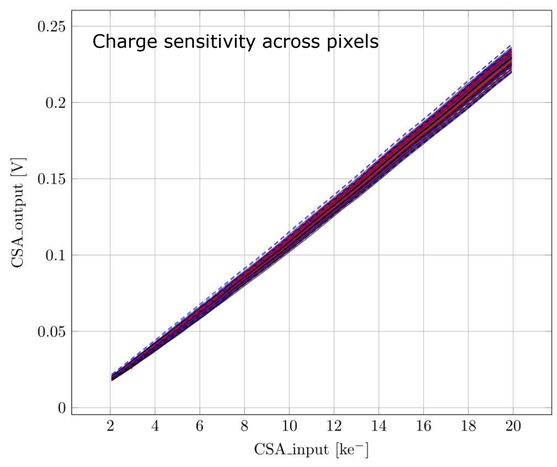
### Charge sensitive amplifier

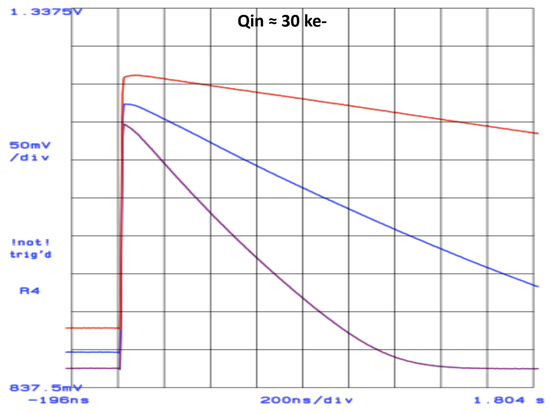



- **Regulated cascode design**
- **Active feedback transistor Mf:**
  - 1/gm resistor for small signals
  - Constant current source for large signals
  - M1 provides a DC path for the detector leakage current
  - Ri + Ci ensure low-frequency operation of the leakage compensation circuit
- **Power consumption** @ 1.2 $V_{DD}$ = 4.8 μW

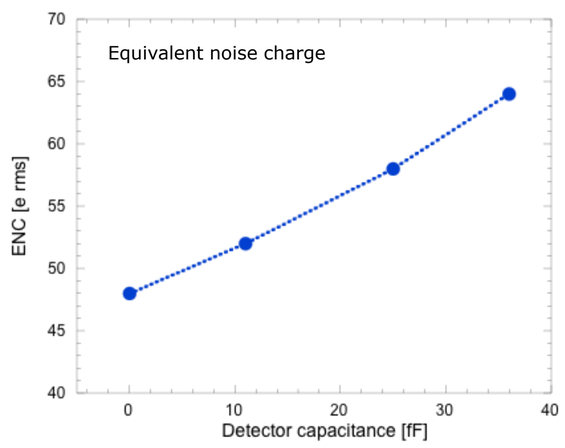



Preamplifier output response for small and large signals




Effect of Id feedback current on the preamplifier response

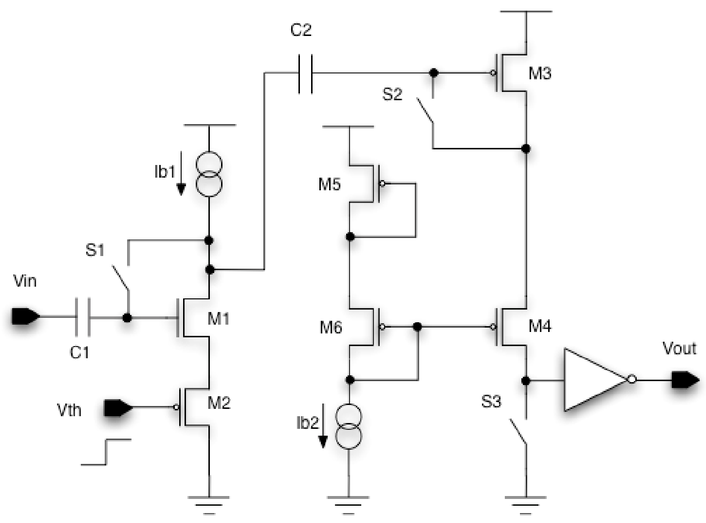



- ≈ 5 ns **rise time** @ $Q_{in}$=750 $e^-$
- **Changing slope** by adjusting the preamplifier Id feedback current
- **Charge sensitivity G** (evaluated on 256 pixels):
- $G_{mean}$ = 11.0 mV/$ke^-$
- $\sigma_G$ = 0.21 mV/$ke^-$
- **Equivalent noise charge** (ENC) smaller than 70 $e_{rms}$ for a preamplifier input capacitance $C_D$ =35 fF

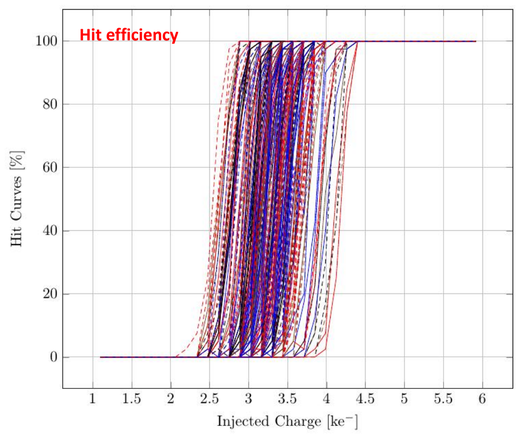
**From circuit simulations:**

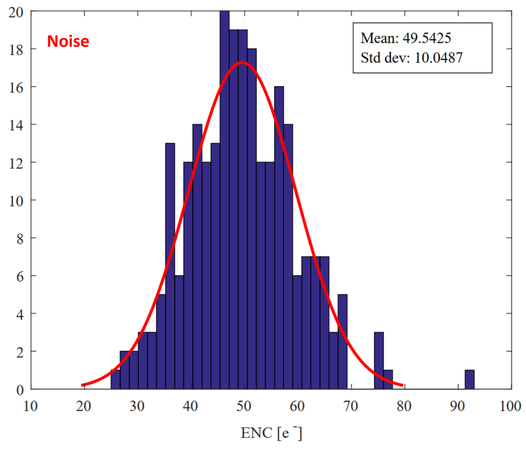
- **Leakage compensation** circuit for leakage currents up to 14 nA
- Regulated cascode forward gain stage:
  - DC Open Loop gain → 53 dB
  - Cutoff frequency → 2.3 MHz

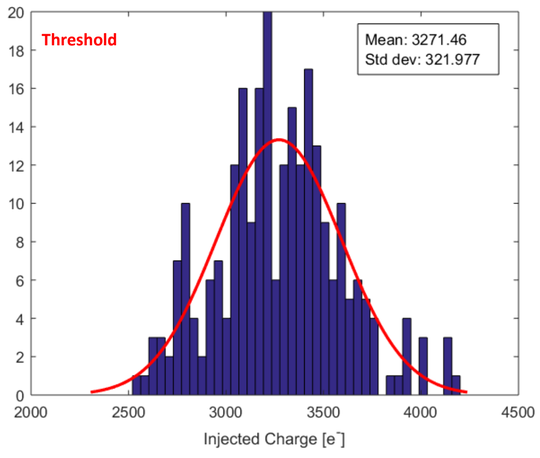
### Comparator




Operated in two different phases:
**reset phase** → the comparator gets reset and a proper bias is provided to the two stages – S1, S2, S3 closed
**active phase** → an active comparison takes place by injecting both the input and the threshold signals Vth at the comparator inputs – S1, S2, S3 open




- Comparator able to detect **hits in two consecutive bunch crossing periods**
- **Noise and threshold dispersion** data extracted from the hit efficiency curves
- **Equivalent noise charge** ENC → 50 $e_{rms}$ ($\sigma_{ENC}$ =10 $e_{rms}$)
- **Threshold dispersion** close to 320 erms, **significantly higher** than expected → bad simulations settings for the comparator's second stage. Re-design needed