Contribution ID: **113** Type: **Poster**

# Design and Test of a 65nm CMOS Front-End with Zero Dead Time for Next Generation Pixel Detectors

*Tuesday, 12 September 2017 17:45 (15 minutes)*

This work is concerned with the design of a synchronous analog processor with zero dead time developed in a 65 nm CMOS technology, conceived for pixel detectors at the HL-LHC experiment upgrades. It includes a low noise, fast charge sensitive amplifier with detector leakage compensation circuit, and a compact, single ended comparator able to correctly process hits belonging to two consecutive bunch crossing periods. A 2-bit Flash ADC is exploited for digital conversion immediately after the preamplifier.
A thorough discussion on the design and on the characterization of the readout channel will be provided in the conference paper.

## Summary

Next generation pixel chips at the HL-LHC will operate with extremely high particle rates and radiation levels. In the so-called phase 2 upgrade, ATLAS and CMS will need a completely new tracker detector complying with the very demanding operating conditions and the delivered luminosity (up to 5x10ˆ34 cmˆ-2sˆ-1 in the next decade). Very low noise performance of the analog front-end, along with stable low threshold operation, will be key points for the new chips in order to be highly efficient.
The 65 nm CMOS technology has been chosen by the designer community for the development of future readout chips at the HL-LHC. This technology retains the good degree of tolerance to ionizing radiation that is typical of CMOS processes in the 100 nm regime and enables the integration of advanced in-pixel analog and digital functions.
A synchronous analog front-end with zero dead time, called IFCP65, has been designed in a 65 nm CMOS technology in the framework of the CERN RD53 collaboration. It includes a low noise, fast charge sensitive amplifier with detector leakage compensation, and a compact, single ended comparator able to correctly process hits belonging to two consecutive bunch crossing periods. A 2-bit flash ADC is exploited for the analog-to-digital conversion.
The analog processor includes a charge sensitive amplifier (CSA) based on a regulated cascode gain stage and featuring a leakage current compensation circuit able to deal with the radiation-induced increase in the detector leakage. The output response of the CSA, whose measured charge sensitivity is close to 10 mV/ke, is characterized by a fast rising edge (a few nanoseconds), with an overall current consumption of the stage close to 4μA. The equivalent noise charge measured at the preamplifier output is close to 65 electrons for a 35 fF detector capacitance. The signal at the CSA output is fed to the threshold discriminator with auto-zero capability, which provides hit/no-hit information at the channel output. It is operated in two different phases, lasting 12.5 ns each: in the first one, called reset phase, the comparator gets reset and a proper bias is provided to the two stages making up the comparator. During the second one, an active comparison takes place by injecting both the CSA output and the threshold signals at the comparator inputs.
A 2-bit flash ADC is exploited for digital conversion immediately after the charge sensitive amplifier. The ADC design is based on three comparators with the same architecture used for the hit comparator, resulting in a conversion time for the in-pixel ADC equal to 12.5 ns. The ADC can be turned off, thus enabling a pure binary operation of the readout channel.

A thorough discussion on the design and on the characterization of the readout channel, included in a prototype chip integrating an 16x16 pixel matrix, will be provided in the conference paper.

**Primary authors:** GAIONI, Luigi (University of Bergamo); BRAGA, Davide (FERMILAB); CHRISTIAN, David (Fermilab); DEPTUCH, Grzegorz (Fermi National Accelerator Lab. (US)); FAHIM, Farah (Fermilab); NODARI, Benedetta (Institute of Nuclear Physics (IPNL), CNRS/IN2P3, Lyon, France); RATTI, Lodovico (University of Pavia); RE, Valerio (University of Bergamo); ZIMMERMAN, Thomas (Fermi National Accelerator Lab. (US))

**Presenter:** BRAGA, Davide (FERMILAB)

**Session Classification:** POSTER Session

**Track Classification:** ASIC