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A Monolithic HV/HR-MAPS Detector with a Small Pixel Size of 50 µm x 50 µm for the ATLAS Inner Tracker Upgrade

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This paper presents a HV/HR-MAPS detector designed in the framework of the HVCMOS collaboration for the ATLAS Inner Tracker update in the HL-LHC era. It was fabricated with a 150 nm HVCMOS process which includes a layer to isolate the bulk of PMOS transistors from the collecting node of the sensor. All front-end electronics are integrated inside the pixel, which is of only 50 µm x 50 µm, and include a preamplifier, a shaper, a discriminator and a digital block with FEI3 column drain architecture. Experimental results will be presented.

Summary

Monolithic pixel detectors, built by means of a deep-n-well over a high resistivity p substrate and reverse biased at a high voltage, present a large depletion region. This yields to fast charge collection and moderate levels of radiation hardness, around 1e-15neq/cm2. Such performances and a moderate fabrication cost has turned the interest of several groups on developing some demonstrators for the 5th layer of the upgrade of the Inner Tracker detector of ATLAS for the HL-LHC era.

In this contribution will be presented a small demonstrator of 5.0 mm x 2.5 mm fabricated with a 150 nm process from LFoundry. The pixel matrix occupies 3.9 mm x 2 mm of the total area and it is composed of 40 rows and 78 columns with a pixel size of only 50 µm x 50 µm. In such a small area the analog and digital front-end electronics have been integrated. The inclusion of a CMOS discriminator and digital gates in pixel was possible by using an isolation layer that avoids punch through between the n-wells and the deep n-well (collecting node of the sensor).

The matrix has four different pixel flavours distributed in 2 submatrices of 40 rows and 20 columns and another two of 40 rows and 19 columns. The differences between the flavours are on the analog front end electronics. These are composed of preamplifier, shaper, and CMOS discriminator. The feedback capacitor was implemented in two different ways. In the first one no isolation layer was placed under the preamplifier so the bulk of the PMOS transistors is shorted to the collecting node (deep n-well). The drain-bulk capacitance of the PMOS output transistor is used as the feedback capacitor. In the second one the isolation layer was placed under the preamplifier and a MIM feedback capacitor was used. Two variants were implemented for these two pixels flavours, one with linear transistors and the other with circular transistors.

The function of the digital front-end electronics is to capture the time stamp for the leading edge and trailing edge transitions of the discriminator when a hit is detected. This information is stored in a 16-b DRAM memory. The layout was made full custom in order to integrate all the electronics in the given area. Each hit pixel contains 22 bits of information to be read out: 16 bits for the time stamp information and 6 bits for the address. This information is sent from the pixel that has detected a hit through a 22-b bus to an End Of Column (EOC) cell where it is stored temporarily. The EOC cells form a shift register which is read continuously by a control unit at 40 MHz. This passes the data to 2 serializers which transmit the information at 640 MHz through LVDS ports. The readout is asynchronous and with no trigger.

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