Prototype chip for a control system in a serial powered pixel detector at the ATLAS Phase II upgrade

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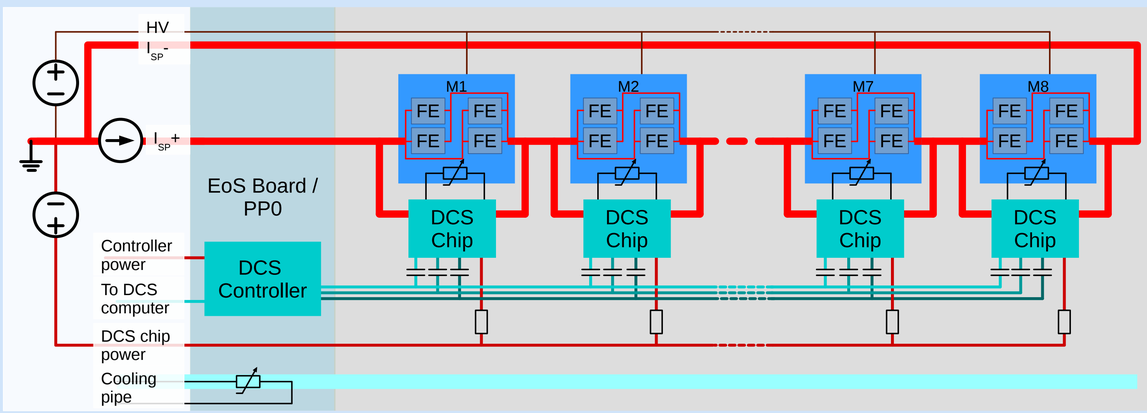
Niklaus Lehmann[1*], Rizwan Ahmad[2], Philip Bergmann[1], Tobias Fröse[2], Michael Karagounis[2], Susanne Kersten[1], Peter Kind[1], Yann Narbutt[1], Jakob Schick[1], Christian Zeitnitz[1]

[1]University of Wuppertal, [2]FH Dortmund

Abstract: A new inner tracking detector (ITk) for the Phase-II upgrade of the ATLAS experiment is in development. A serial power scheme is foreseen for the pixel detector. This requires a new detector control system (DCS) to monitor and control the pixel modules in the serial power chain. The Pixel Serial Power Protection (PSPP) chip is an ASIC for this purpose. It operates parallel to the modules and contains an ADC and bypass transistor. This poster presents test results for the DCS chip and all its prototyped components. It includes irradiation up to 600 Mrad and stability measurements.

Serial Power Chain

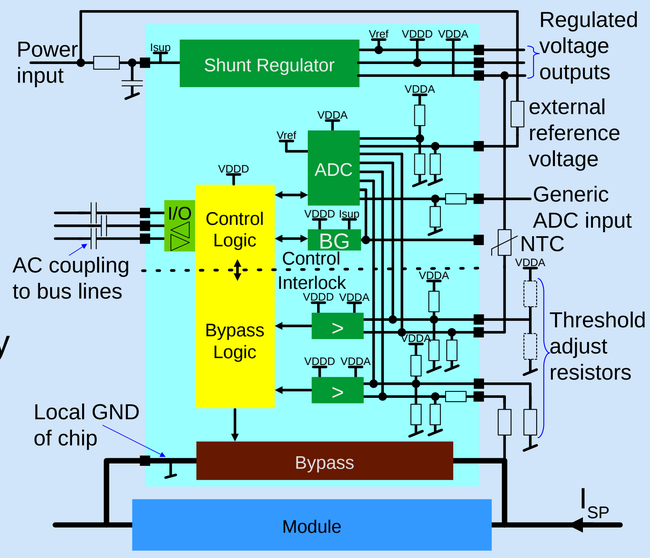
- Serial power chain to reduce cables
- Constant current through all modules
- Individual reference voltage for modules
- Single module failure affects whole chain
- DCS chip parallel to each module
- Constant monitoring of module and deactivation in case of failure
- Independent operation of DCS elements



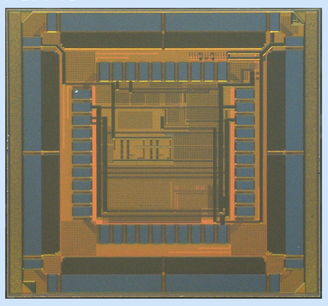
DCS Chip Prototype: PSPP and PARC

Pixel Serial Power Protection chip (PSPP)

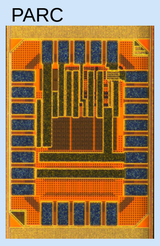
- Radiation hard bypass transistor for 8 A
- Automated bypass activation
- Operation in serial power chain
- Serial Control Bus (SCB): dedicated communication over single ended AC coupled lines
- Logic with triple modular redundancy



PSPPv3

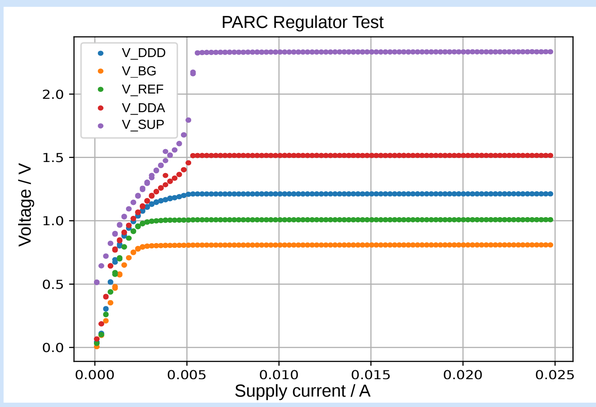


PARC



PSPP Add-on Regulator Comparator chip (PARC)

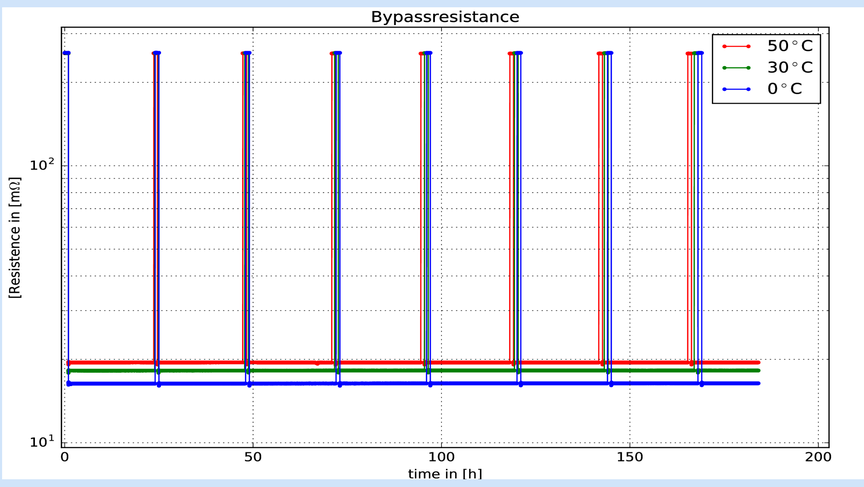
- Add-on chip with remaining rad-hard elements of the DCS chip
- Radiation hard shunt regulator and LDO regulators
- Radiation hard comparator
- Test logic for SEU measurements



Longterm Tests

A single PSPPv3 was tested in a climate chamber at different temperatures, each for 7 days of continuous operation

- Operated at 0 °C, 30 °C and 50 °C
- Bypass activated for 23 h and deactivated for 1 h
- 3 A serial current applied during the whole time



Bypass

- On-resistance stable over time
- On-resistance increases with temperature
- $R_{ON@0°C}$ = 16.37 ± 0.02 Ω
- $R_{ON@30°C}$ = 18.22 ± 0.01 Ω
- $R_{ON@50°C}$ = 19.48 ± 0.13 Ω

Logic

- Stable communication during entire test duration
- No error in registers detected

ADC

- Constant value measured : 557 ± 3 mV
- Error smaller than 50 mV compared to volt meter

Detector Control System

Interlock path

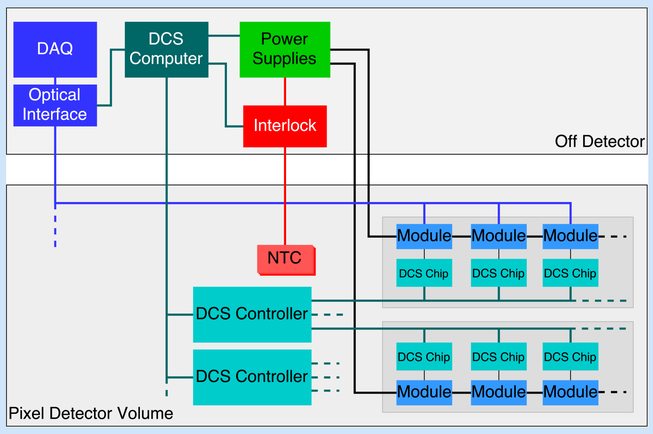
- Hardwired
- Independent
- Permanently running

Control path

- Independent communication
- Monitor and control on module level

Diagnostics path

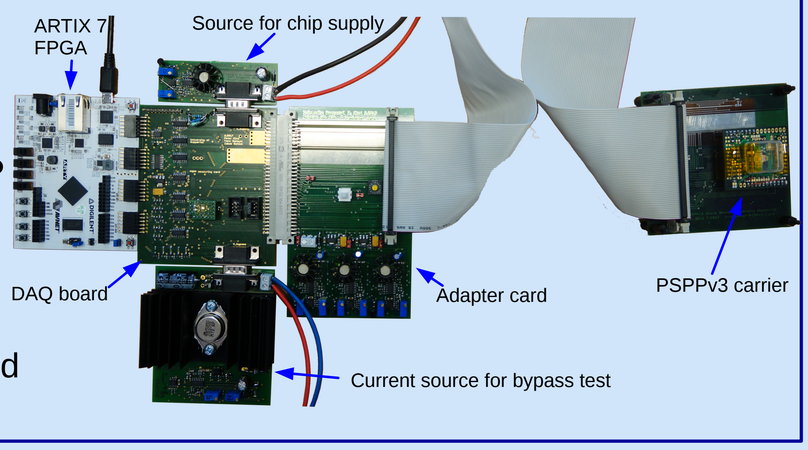
- Through readout
- Front End (FE) information



Test Setup

FPGA based test system

- DAC and ADC to generate and measure analog signals of the PSPP
- Communication with PSPP
- Control of digital signals
- Python based control program
- Different adapter boards
  - For testing with probe card
  - For irradiation tests



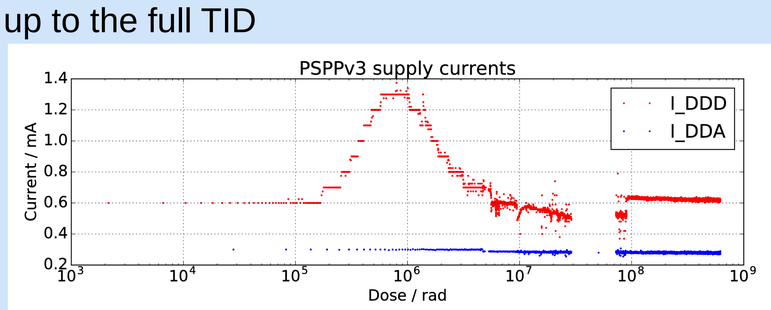
Irradiation Tests

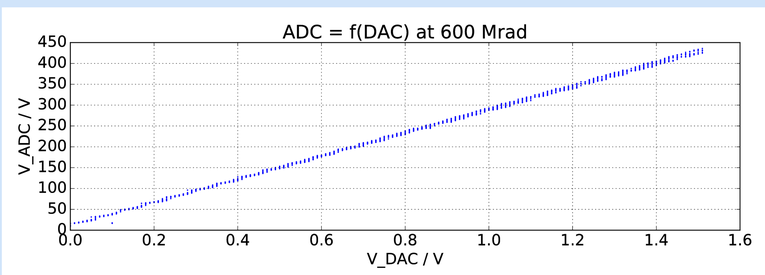
The PSPPv3 and PARC chips were irradiated with a X-Ray machine up to a total ionizing dose (TID) of 600 Mrad

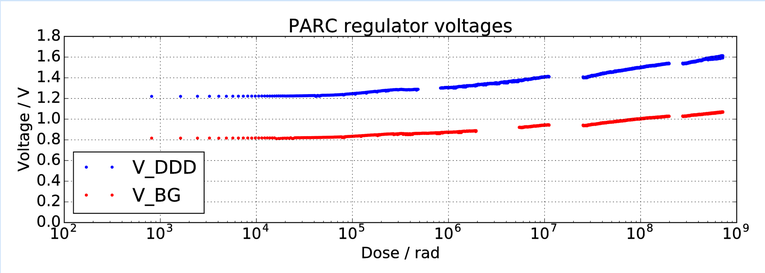
- First 10 Mrad with lower dose rate of 235 krad/h
- Afterwards with 3.2 Mrad/h up to the full TID

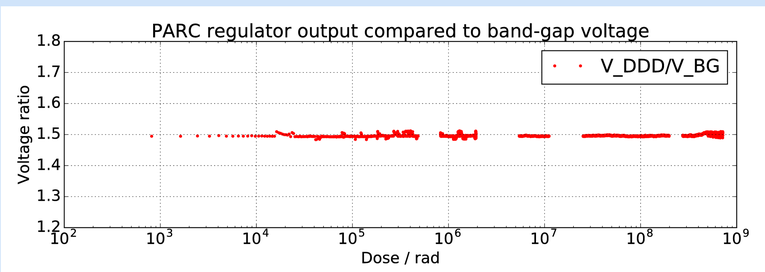
PSPPv3 irradiation

- Observed expected rise in digital current at 1 Mrad for used technology
- Stable communication during the test
- ADC working and stable readout for the entire TID
- Bypass operational after irradiation
- R_{ON} increased by 6 mΩ







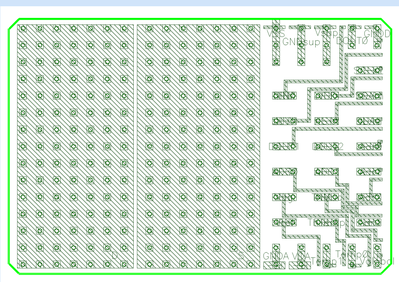


PARC irradiation

- Drift in the band-gap observed
- Comparator working during entire irradiation
- Oscillating behavior observed at a small input difference (< 50mV)
- Regulators operating throughout full irradiation

Outlook

- Additional characterization measurements of the PARC regulators are planned
- Next prototype v4 in development
  - Merge of PSPPv3 and PARC
  - Fix of observed problems
  - Change from wirebonds to bump bonds
  - Submission in Nov 2017



Padframe proposal for PSPPv4