Contribution ID: **32** Type: **Poster**

Prototype Chip for a Control System in a Serial Powered Pixel Detector at the ATLAS Phase II Upgrade

Tuesday 12 September 2017 17:45 (15 minutes)

A new inner tracking detector (ITk) for the Phase-II upgrade of the ATLAS experiment is in development. A serial power scheme is foreseen for the pixel detector. This requires a new detector control system (DCS) to monitor and control the pixel modules in the serial power chain.
The Pixel Serial Power Protection (PSPP) chip is an ASIC for this purpose. It operates parallel to the modules and houses an ADC and bypass. This talk presents test results with the PSPPv3 chip. It includes irradiation up to 500Mrad and investigations of a serial power chain with up to 8A supply current.

Summary

The upgrade of the LHC to the High-Luminosity LHC requires improved detectors. A completely new full-silicon tracker is in development for the ATLAS Phase-II upgrade. This tracker includes a pixel part with about 10 times more modules than the current version. A serial powering scheme to reduce the number of service lines to the detector is the baseline. A new detector control system (DCS) is required for a save operation over the planned life time of 10 years.
The current concept envisions three parallel paths for the DCS. The security path is a hardwired interlock system. This path doesn't need any software or interaction and acts as last line of defense. The diagnostics path provides information on demand. It is merged with the regular data readout and provides the highest granularity and most detailed information. The control path is used to supervise the entire detector. This path has its own communication lines independent from the regular data readout for reliable operation.
The main elements in the control path are the DCS chip and controller. The DCS chip operates in the serial power chain parallel to the pixel modules. This imposes different operating voltages of each DCS chip in the chain. Additionally, they should be powered independent of the serial supply current. A power scheme is proposed which uses only one additional service line for the operation of the DCS chip. Each chip monitors one module and has capabilities to bypass the module. This guarantees operation of the serial chain if the module fails. The DCS chip communicates through a dedicated communication path with the controller chip. These communication has to operate with each DCS chip on a different voltage. This is realized with single ended AC coupled lines and specially developed I/O drivers. The controller receives commands by CAN from the DCS computers.
In this talk, we explain the pixel serial power protection (PSPP) chip, a prototype for the DCS chip. The third version, called PSPPv3, was designed to respect the updated power requirements and has capabilities to bypass up to 8 A. The other components in the chip are an ADC for measuring the module voltage and temperature, a communication logic implemented in triple modular redundancy (TMR) and comparators for a local module interlock. The bypass is activated automatically if the temperature or voltage go over a fixed threshold. We show results of test in the serial power chain and the operation of the PSPPv3.
The DCS chip will observe the same radiation levels as the pixel modules. Currently they are designed to work with a total ionizing dose (TID) up to 500 Mrad. We present results of irradiation tests with the PSPPv3 chip.

Primary authors: KARAGOUNIS, Michael (FH Dortmund); KERSTEN, Susanne (Bergische Universitaet Wuppertal (DE)); LEHMANN, Niklaus (Bergische Universitaet Wuppertal (DE)); ZEITNITZ, Christian (Bergische Universitaet Wuppertal (DE))

Presenter: LEHMANN, Niklaus (Bergische Universitaet Wuppertal (DE))

Session Classification: POSTER Session

Track Classification: ASIC