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Performance of the CATIA ASIC, the APD Readout Chip Foreseen for the CMS Barrel ECAL Electronics Upgrade at the HL-LHC

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The CMS ECAL barrel electronics will be upgraded for the HL-LHC to meet the latency and bandwidth requirements of the Phase-II Level-1 trigger system. The front-end electronics will mitigate the increasing noise from the avalanche photodiodes (APDs), discriminate against anomalous APD signals and provide improved timing information. The foreseen solution is to replace the current Charge-Sensitive-Amplifier with a Trans-Impedance Amplifier (TIA) which should provide the extra bandwidth needed to maintain the integrity of the detector signal shape. The first ASIC prototype, called CATIA, has been successfully designed in TSMC 130 nm CMOS technology and its test results will be presented.

Summary

The LHC Phase-II upgrade will lead to a significant increase in luminosity which implies the full replacement of the ECAL Barrel (EB) electronics to meet the Level-1 trigger requirements. By including the front-end electronic in this upgrade, there is a possibility to mitigate the increasing noise induced by avalanche photodiode (APD) ageing, to improve the suppression capability of APD anomalous signals and to reach the intrinsic timing resolution of the detector constituted by crystals and APDs, in order to help to discriminate between energy deposits coming from different overlapping events. This can be done by replacing the actual APD readout chip (MGPA) based on a Charge Sensitive Amplifier (CSA) with a high speed Trans-Impedance Amplifier (TIA) - 50 MHz of bandwidth - followed by 160 Msps 12-bit ADCs. The high speed TIA and high speed ADC will enable the discrimination of spike signals from the scintillation signals by analyzing the characteristic differences of their shapes (width measurement). In addition, they will provide time measurements at the level of 30 ps for electrons and photons above 50 GeV. The architecture of the TIA is a Regulated Common-Gate (RCG) TIA which offers a reduced input resistance compatible with the high input capacitance (200 pF) of the APD providing the high bandwidth foreseen. The gain is achieved by a resistor chosen to fit the maximum input signal at 2TeV for an INL < +/- 0.1%. The output dynamic is split into 2 ranges: 200 GeV & 2 TeV. The 200 GeV is achieved through a gain10 stage after the TIA.

The first step of this electronics upgrade is to design this TIA independently of the ADC to confirm the simulation study results and to analysis the performances obtained with the TSMC 130 nm process. This was achieved by prototyping an ASIC called CATIA formed by 2 different channels realized in the 2 voltage supplies allowed by the process, 1.2V and 2.5V, for 4 channels in total. The difference between channels comes from the architecture of the gain10 stage which permits to define or control the internal DC voltage level.

The chip was submitted in October 28 2016 and received in the end of February 2017. The tests performed in laboratory with pulse generators and an APD detector confirm the functionality of the chip and the performances obtained prove that the TIA is a good candidate for the ECAL Barrel electronics HL-LHC upgrade.

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