LAPA, a 5 Gb/s modular LVDS driver in 180 nm CMOS with capacitively coupled pre-emphasis

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Abstract

A pseudo-LVDS driver has been designed in the Tower Jazz 180nm technology for operation up to 5 Gb/s.
It contains parallel main driver units, based on an H-bridge circuit steering a current into an external load. The number of active units is selectable to reduce switching capacitance and static current, and hence power consumption, if a smaller current swing can be tolerated. Pre-emphasis is applied with a capacitively coupled charge-injection circuit. In nominal condition with a steering current of 4 mA over a 100 Ω termination resistor it consumes 30 mW from a 1.8 V supply.

ATLAS ITk upgrade

The ATLAS experiment at CERN plans to upgrade its Inner Tracking system (ITk) for the High-Luminosity LHC in 2026 [1], with an increase of

- luminosity from $1x10^{34}$ $cm^{-2}s^{-1}$ to $7.5x10^{34}$ $cm^{-2}s^{-1}$.
- Interactions from 50 pp to 200 pp per bunch crossing.

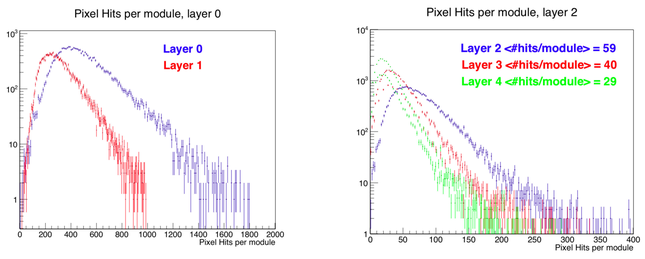


Fig. 1: Simulated pixel hits per module for different layers of the Itk upgrade. Pixel size 50x50x (150µm depletion).

MALTA CHIP

After the ALPIDE monolithic sensor was successfully implemented in the TowerJazz 180nm CMOS imager technology [2], and promising irradiation results were obtained modifying this process [3], an ATLAS-specific development in this modified process was started. The MALTA (Monolithic from ALICE to ATLAS) chip is being submit in and will be tested later in 2017.
Its many features are

- 512x512 pixel matrix with 36.4µm pitch.
- 1 µW frontend with in-pixel discrimination.
- Full asynchronous readout.
- Side CMOS output pads for chip to chip data communication.
- 40 LAPA (pseudo-LVDS driver for the Atlas Pixel Apparatus) drivers.

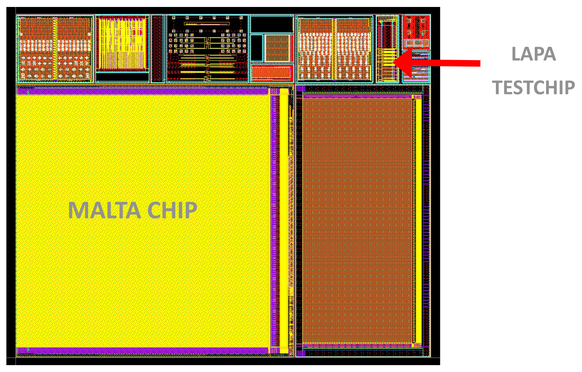


Fig. 2 : Reticule of the submission to TowerJazz.

LAPA TEST CHIP

The test chip has been designed to test the LAPA pseudo-LVDS that is integrated into MALTA chip. It contains 10 data transmission channels with:

- CMOS/ LVDS selectable input.
- CMOS/LVDS selectable output.
- Output common mode feedback lock.
- Selectable input 100 Ω termination resistor.

The chip operates at 1.8 V.

SPEC	Min	Max	Nom
LVDS IN VCM	0.8 V	1 V	0.9 V
LVDS IN Vdiff	0.3 V	-	0.4 V
LVDS IN T Res	-	-	100 Ω
LVDS IN bit rate	-	5 Gbit/s	-
CMOS IN bit rate	-	5 Gbit/s	-
CMOS OUT bit rate	-	2 Gbit/s (0.5pF load)	-
LVDS OUT VCM	-	-	0.9 V
LVDS OUT Vdiff	-	-	0.4 V
LVDS OUT Iout	0.8 mA	6 mA	4 mA
LVDS OUT T Res	-	-	100Ω
LVDS OUT bit rate	-	5 Gbit/s (1pF load)	-

Tab. 1: LAPA test chip design specifications.

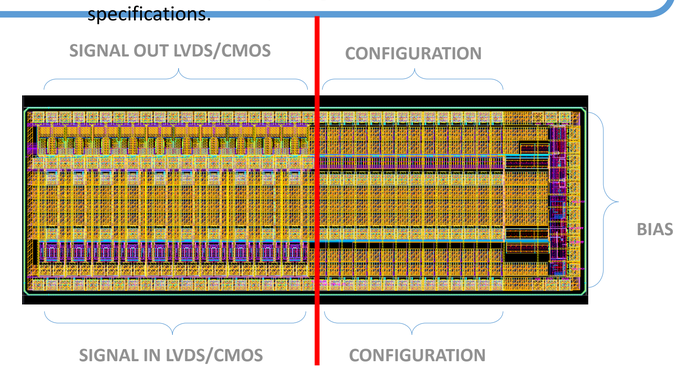


Fig. 3 : LAPA test chip layout.

Main driver

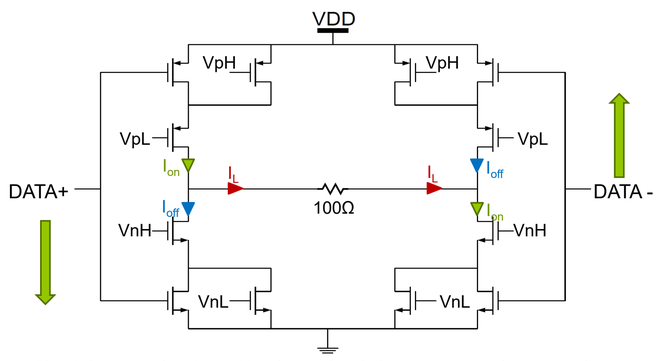


Fig. 4 Schematic of the H-bridge circuit implemented in the main driver with the representation of a switching event.

The main driver is based on a H-bridge steering the current into the external output load. Each half branch of the H-Bridge is a three transistors circuit acting as a switchable current source.

- A switch limits the half branch current to I_{on} or I_{off}.
- I_{on} and I_{off} are defined by [V_{nH} V_{pL}] and [V_{nL} V_{pH}].
- I_{on}- I_{off} defines I_L.

The design is optimised to generate 400 mV over a 100 Ω termination resistor using a 4 mA current, with a common mode voltage of 0.8 V.

Common mode feedback

The driver is optimized to operate with a 400mV differential output voltage, with a nominal common mode voltage (VCM) equal to 0.8V.
The ON current I_{on} of the PMOS can be regulated in an arbitrary number of main driver units using a feedback amplifier that locks the VCM at the nominal value.

LAPA pseudo-LVDS driver

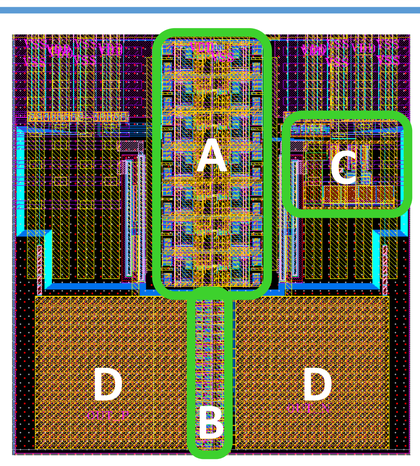


Fig. 5 Layout of an LAPA output driver. A – H-bridges of the main driver. B – Pre-emphasis drivers. C – common mode feedback amplifier. D – Output pads.

Pre-emphasis

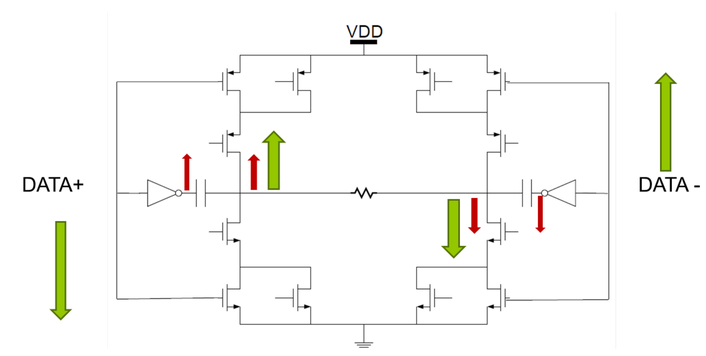


Fig. 6 Schematic of the pre-emphasis circuit, with the representation of a switching event.

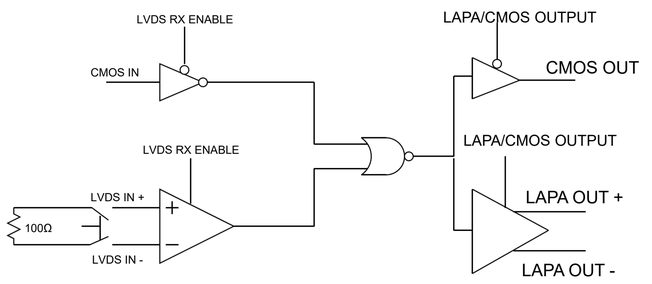
Speed can be improved applying pre-emphasis (PE) with a capacitively-coupled charge injection circuit with the following features:

- 16 independent capacitively-coupled charge injection circuits.
- Each PE circuit drives 25 fF capacitor.
- Tunable PE strength, selecting the number of active drivers, to optimize the performance in terms of speed and dynamic power consumption, depending on the external load.
- Optimized layout to reduce the parasitic capacitance of the buffering driving node and the overall pad capacitance.
- No need of a clock to operate the pre-emphasis.

Data transmission channel

Each one of the ten channels of the LAPA chip presents:

- CMOS/ LVDS input, configured per chip.
- CMOS/LVDS out selection with on chip bonding.
- Shared data path between CMOS/LVDS input output.
- Dedicated power supply pad for input and output.



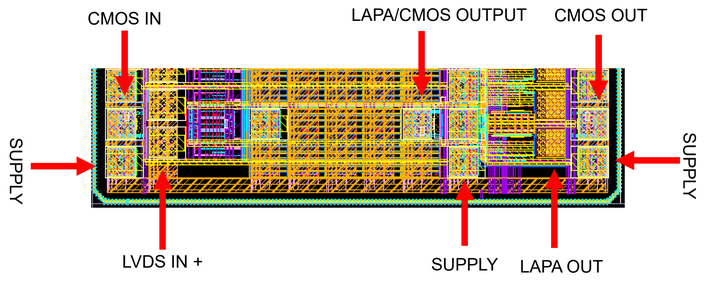


Fig. 7 Simplified schematic and layout of a data transmission channel.

Test and application

LAPA will be tested applying a 5 Gbit/s signal to the LVDS channel. The flexible configuration of the output driver will allow minimizing the power consumption to achieve the desired performance.

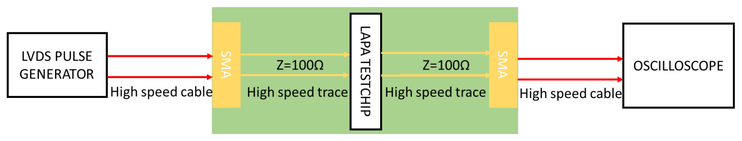


Fig. 8: Schematic of the measurement setup for the LAPA test chip.

The next iterations of the Tower Jazz monolithic pixel developments will aim to push the output speed to 5Gbit/s, fully exploiting the capabilities of LAPA. The plan is to aggregate the data coming from four detectors to a single LVDS output that communicates with the external world.

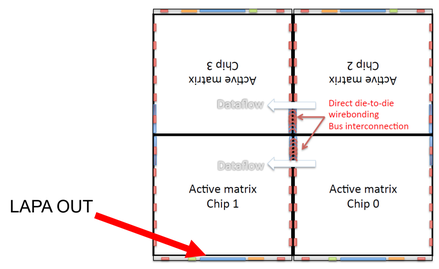


Fig. 9: Four- chip communication schema.

Simulated performance

In the Fig. 10 is shown the simulated eye diagram of the pseudo-LVDS output. The input signal is injected in the LVDS receiver, with a common mode voltage of 0.8 V and a differential voltage of 400 mV. The expected peak to peak jitter is around 45ps.

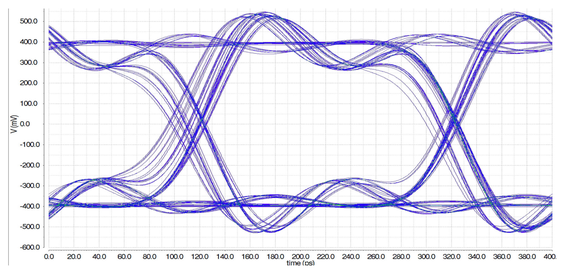


Fig. 10 : Eye diagram of a simulated 2.5GHz signal, transmitted in a LVDS channel of the LAPA test chip. Simulated peak to peak jitter of 45 ps.

Acknowledgements & References

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[1] S.McMahon et al. , "Initial Design Report of the ITk: Initial Design Report of the ITk",CERN,cATL-COM-UPGRADE-2014 29], Oct2014, https://cds.cern.ch/record/1952548
[2] D. Kim et al., JINST 12 (2016) C02042
[3] W. Snoeys et al., NIM A 871C (2017) pp. 90-96, DOI: 10.1016/j.nima.2017.07.046