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LAPA, a 5 Gb/s Modular LVDS Driver in 180 nm CMOS with Capacitively Coupled Pre-Emphasis

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A pseudo-LVDS driver has been designed in a 180 nm technology for operation up to 5 Gb/s.
It contains parallel main driver units based on an H-bridge circuit steering a current on an external load. The number of active units is selectable,
to reduce switching capacitance and static current, and hence power consumption, if a smaller current swing can be tolerated.
Pre-emphasis is applied with a capacitively coupled charge-injection circuit. In nominal condition with a steering current of 4 mA over a 100 Ω termination resistor it consumes 30 mW from a 1.8 V supply.

Summary

The ATLAS experiment at CERN plans to upgrade its Inner Tracking system (ITk) for the High-Luminosity LHC in 2026 [1]. After the ALPIDE monolithic sensor was successfully implemented in the TowerJazz 180nm CMOS imager technology [2],
and promising irradiation results were obtained modifying this process [3], an ATLAS-specific development in this modified process was started. As part of the development a 5 Gb/s LVDS driver has been designed. This driver is used both in a full pixel matrix prototype MALTA (Monolithic pixel sensor from ALICE to ATLAS), and in a specific test chip LAPA (pseudo-LVDS driver for the Atlas Pixel Apparatus). The MALTA chip contains 40 parallel drivers, and LAPA 16.

The LVDS driver contains a main driver and a pre-emphasis circuit.

The main driver is based on a H-bridge scheme that steers the current on the external output load. Each half branch of the H-Bridge has a three transistor circuit that act as a switchable current source.
The transistor defining the OFF current Ioff is in series with the transistor defining the ON current Ion. Another transistor, operated as a switch, is in parallel with the transistor defining the OFF current. When the switch is in the OFF state, the output current is limited to Ioff, and when it is ON, the output current is limited to Ion. This scheme avoids a current source in series with the H-bridge, resulting in a larger operating margin above saturation, allowing a reduction in transistor size (width) and hence dynamic power consumption.

The main driver consists of seven driving units operating in parallel. The number of active units can be varied to adapt the circuit switching capacitance to allow the required static current, hence optimizing the dynamic power consumption. The design is optimised to generate 400 mV over a 100 Ohm termination resistor using a 4 mA current. Under these conditions, the expected power dissipation to transmit a 2.5 GHz clock signal is approximatively 30 mW.

Speed performance can be improved applying pre-emphasis with a capacitively-coupled charge injection circuit.
LAPA integrates 16 independent capacitively-coupled charge injection circuits, of a which an arbitrary number can enabled to vary the pre-emphasis according to the need. Each circuit consist of a CMOS buffering stage that drives a coupling capacitance of 25 fF. The layout is carefully optimized to reduce the parasitic capacitance of the buffering driving node and the overall pad capacitance. The pre-emphasis strength is so tunable in order to optimize the performance in terms of speed and dynamic power consumption, depending on the external load of the driver.

A common mode feedback circuit holds the common mode to about 800 mV, but this circuit can be disabled if the common mode voltage is set externally.

Main driver current biases can be adjusted using four bits on-chip digital-to-analog converters, with a total maximum output current of 6.4mA.

LAPA is embedded in MALTA chip. A separate test chip implements 16 LAPA drivers, with CMOS and LVDS input-output pads, for a detailed characterization.

Results and measurements will be presented.

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