A micropower readout ASIC for pixelated liquid Ar TPCs

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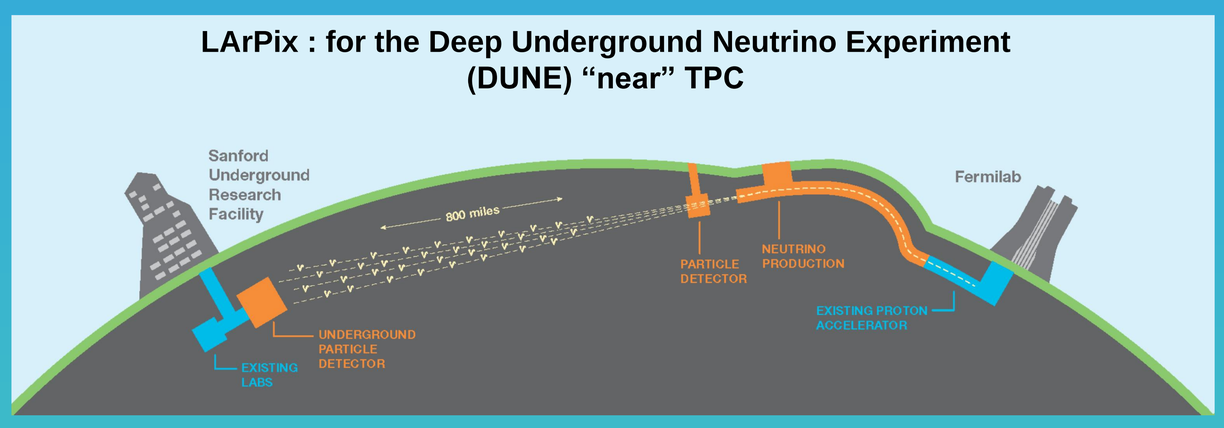
Summary

The motivation for LArPix is to enable large liquid Argon TPCs to record multiple particle interactions per pulse of the neutrino beam. In addition to this increased “hit rate” capability (~ 1 us), another benefit is the reduced trajectory ambiguity achievable with a pixel detector. The feasibility of the pixel sensor array approach has been demonstrated by the LHEP group at U. Bern. The LArPix ASIC seeks to evolve that initial proof of concept towards a working detector system by using a full-custom micropower ASIC solution. A LArPix-based TPC is the primary approach planned for the DUNE near detector.



LArPix ASIC Concept

The design for the LArPix ASIC is similar to many other readout ASICs for capacitive radiation detectors, but requires only a pure integrator as opposed to a shaping amplifier for signal conditioning. This is possible because the noise requirements for the LArPix front end are significantly relaxed owing to the much lower detector capacitance of the pixelated TPC (<4 pF). By comparison, for example, the LARASIC IC must handle the >100 pF load of a wire detector. Removing the shaper not only greatly reduces power dissipation, but also simplifies and accelerates the design of the ASIC.

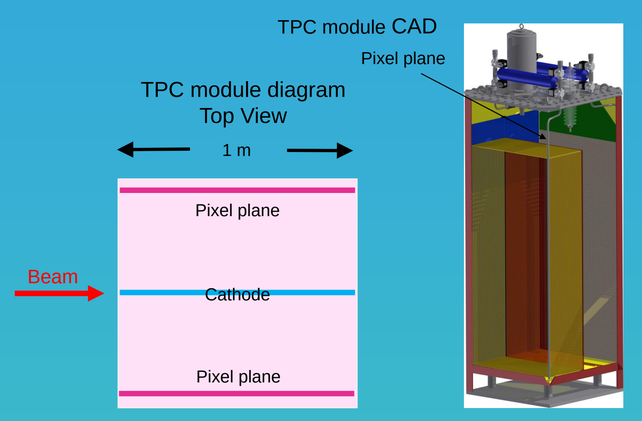
Specification	Value	Units	Note
Number of Analog Inputs (channels)	32 (single-ended)		160 µm effective pitch
Noise (ENC)	300 @ 88K 500 @ 300K	e-	Charge collection estimated at 15 ke- per 1 MIP track in LAr
Channel gain	4 or 45	µV/e-	Digitally programmable
Time resolution	2	µs	with 10 MHz master clock rate
Analog Dynamic Range	~1300	mV	max signal ~250 ke-, minimum detectable signal ~600 e- @ 88 K
ADC resolution	8	bits	programmable LSB, 4 mV nominal (1 ke-)
Threshold Range	0 – 1.8	V	
Threshold Resolution	< 1	mV	nominal
Channel Linearity	1	%	
Operating Temperature Range	88 - 300	K	
Event Memory Depth	2048	memory locations	~8 ms without data loss in case of track normal to pixel plane
Output Signaling Level	3.3	V	
Digital data rate	10	Mb/s	with 20 MHz master clock
Event readout time	5	µs	

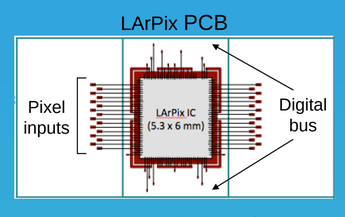
Additional Features

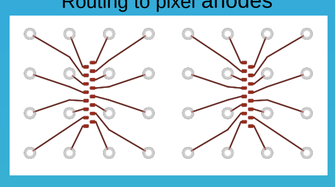
- Front-End Gain select
- Front-End Bypass
- Power Supply Bypass select
- Analog Monitor Bus
- Analog Test Pulse
- Cross-Trigger
- Periodic Reset
- Sampling Pulse Stretching
- ADC Burst
- Channel Mask
- External Trigger Mask

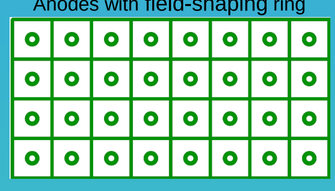
LArPix-based TPC Concept

- Tile a large plane with 32-channel blocks
- ICs daisy-chained atop the digital bus
- Serial pass-thru data transmission reduces cryostat penetrations



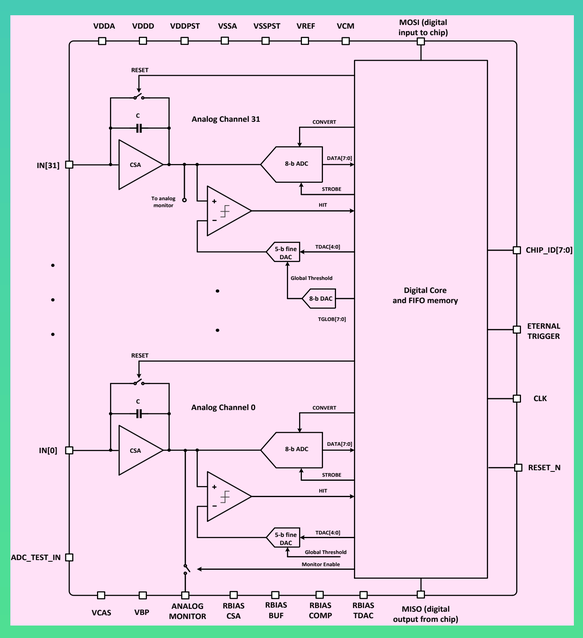






LArPix ASIC Channel

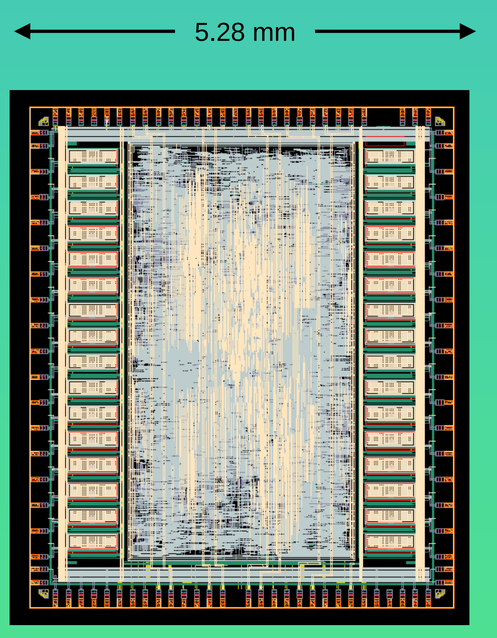
- 32 analog channels
  - Charge Sensitive Amp
  - Discriminator-Schmitt trigger
  - 8-bit global threshold
  - Class-AB Analog buffer
- 8-bit SAR ADC
- Digital Core
  - Chip ID, hit address, 8-bit ADC value, time stamp



Design Challenges

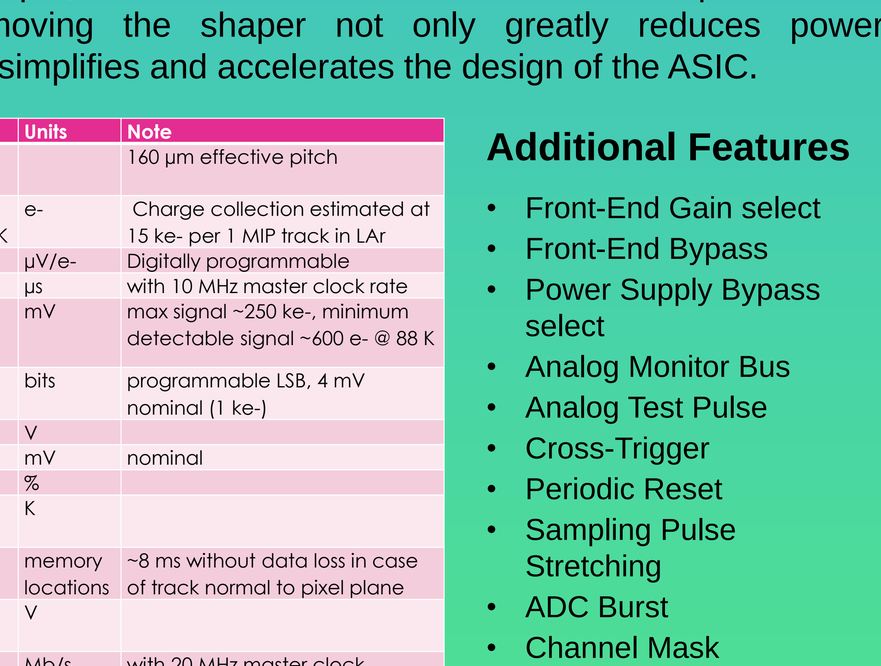
- Increased Vt-mismatch at 88 K
  - 5-bit per-channel threshold trim
- Low power – less than 100 uW/ch
  - Weak Inversion design
  - SAR ADC
- Hot electron damage
  - Non-minimum MOS length*

* Li, Shaorui, et al. "LAr TPC Electronics CMOS Lifetime at 300 K and 77 K and Reliability Under Thermal Cycling", IEEE Transactions on Nuclear Science, vol. 60. no. 6, 12/2013



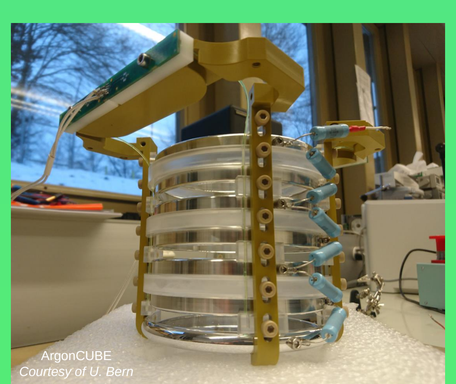
Simulated Operation

- AFE readout of a synthesized event stream
- ~15 ke- event followed by a ~250 ke- event
- Periodic reset, with event reset
- Temperature 300 K and 88 K



Demonstrator TPC setup

- Test in LArPix ‘mini’ ArgonCUBE Pixel Demonstrator TPC provided by U. Bern LHEP group
- High-purity Ar system shared with LUX/LZ dark matter group
- Single-pass LAr purification and cryostat purity seems sufficient for our tests (diffusion length >> detector drift path length)



Status

180 nm RF/Mixed Signal process — Submission June 2017 — Devices due back from fab Sept 2017

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