Contribution ID: **159** Type: **Poster**

# Radiation tolerant serial links for high-speed data transfer in High Energy Physics experiments

*Tuesday, 12 September 2017 17:45 (15 minutes)*

Radiation tolerant serial links for high-speed data transmission in High Energy Physics experiments have been developed at INFN-Pisa and UCSB in a commercial 65nm CMOS technology: 2Gbps Standard-Cell based Serializer and Deserializer and custom 3GHz SLVS Driver and Receiver. Results of test and characterization of the last version of the circuit prototypes produced in the second half of 2016 and tested and characterized, including TID and SEE tests, in the first half of 2017 will be presented. The Serializer and the SLVS Drivers and Receivers have been successfully used in the CHIPIX65-FE ASIC, a demonstrator of a Front-End ASIC for pixel detectors developed at INFN.

## Summary

The increase of the luminosity (up to 5×1034 cm−2 s−1) after the High Luminosity (HL) upgrade of the Large Hadron Collider (LHC) will require the complete re-design of the Front-End (FE) electronics of the inner Silicon Trackers of the LHC experiments because of the new harsh requirements with respect to data rates - up to 5Gbps from each FE ASIC - and radiation tolerance, Total Ionizing Dose (TID) - up to 1Grad - and Single Event Effects (SEE). Since 2014 within the framework of the RD53 collaboration ATLAS and CMS physicists and engineers have been working on the definition of a possible common architecture for the FE ASICs for the future pixel detectors and on the development of serial links that could be used in ASIC development. INFN-Pisa had been already working in collaboration with UCSB in the years 2012-2014 on the design in a commercial CMOS 130nm technology of radiation-tolerant blocks for the implementation of high-speed links. Since 2014 INFN-Pisa joined the RD53 and the INFN CHIPIX65 3-years project whose target was the development of a demonstrator FE ASIC in a CMOS 65nm technology for the readout of future pixel detectors.
We used Standard Cells to implement 20-bit Serializer (SER) and Deserializer (DES) devices, with Triple Modular Redundancy (TMR) to provide protection against SEEs. The Standard Cell approach is still compatible with the required data rates (2Gbps), while a custom design would be required for higher data rates. SER/DES devices provide Data-Strobe (SER) and Data-Valid (DES) output signals that can be used as read and write clocks for buffer FIFOs containing SER input data and DES output data. SER/DES devices have an area of 100um x 56um and 180um x 56um respectively and they dissipate 2.35mW and 17.85mW in typical conditions (T = 25C, VDD = 1.2V).
In the SLVS TX/RX devices the use of thin oxide transistors provides robustness against TID effects while the redundancy of analog building blocks protects against SEEs. In the TX twelve drivers in parallel guarantee SLVS specifications also in case of a radiation-induced error in one of the units. Rising and falling edges of the input signal are detected and used to implement pre-emphasis when this capability is enabled. The RX has a very simple structure based on three two-stage amplifiers in parallel followed by a voting logic. TX/RX dimensions are 130um x 36um and 30um x 16um respectively and absorbed currents are 5.4 mA and 1.3mA in typical conditions.
Final versions of SER/DES and SLVS TX/RX devices have been produced in the second half of 2016. Results of test and final characterization of prototypes, including results of irradiation tests (effects of TID up to 500 MRad and SEE cross-sections evaluated with irradiation with heavy ions) will be presented. SER and SLVS TX/RX devices have been successfully used as building blocks of the CHIPIX65-FE0 demonstrator ASIC. All

the developed circuits are available as components of fully characterized library to ASIC designers.

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**Session Classification:** POSTER Session

**Track Classification:** ASIC