Low Jitter, Radiation Hardened by Design, 2.56 Gbps LVDS/SLVS based Receiver for Analog Time Transmission

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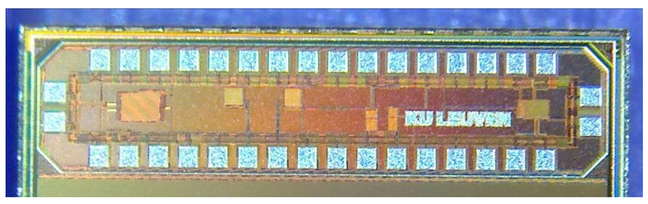
Introduction

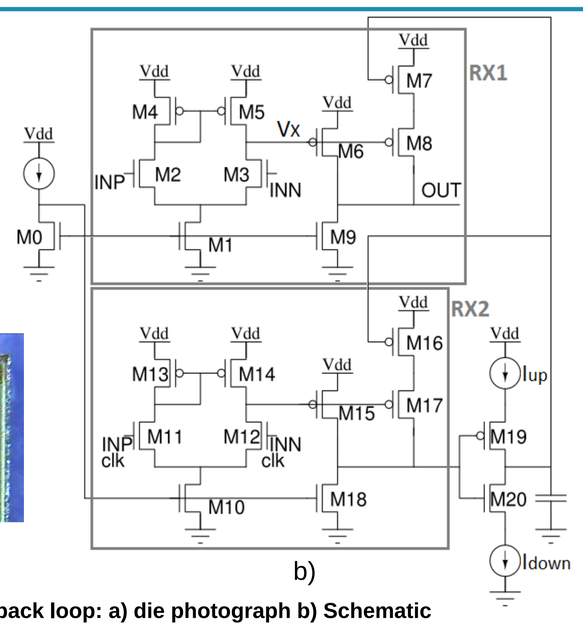
High precision time-domain signal processing circuits like CMS/ATLAS at CERN or laser-ranging sensors, contain information in the time difference between multiple signals or events. In complex systems the distance between the detector and TDC can be rather large, calling for an accurate and long distance transmission of these time-sensitive signals, here done by using LVDS/SLVS signals.

Because the LVDS/SLVS receiver is positioned in the signal path, any introduced timing distortion will cause a measurement error. Consequently, the jitter of the system must be minimized. Secondly, to allow an accurate measurement between multiple events, the rise and fall output delay must remain the same.
This receiver introduces a replica-based feedback loop which uses a 50 % duty cycle input clock to equalize the propagation delays of the rising and falling edges and compensates for the variations introduced by PVT variations and radiation effects.

Schematic



a)



b)

Figure 1: LVDS/SLVS receiver with feedback loop: a) die photograph b) Schematic

- RX1: Accurate timing information
  - Equal propagation delay by balancing M6-M9
- RX2: Replica receiver
  - Compensates PVT and radiation effects.

When Trise = Tfall:
Input: 50 % duty cycle
→ Output 50 % duty cycle
CP: IUP = IDOWN → V_{FB} = VDD/2
Propagation delay asymmetry = duty cycle error
→ duty cycle ≠ 50 %
→ VFB ≠ VDD/2
→ Adjust M7 and M16

Measurement results

- 2.56 Gbps pseudo random input signal / V_{CM} = 0.8 V
- Initial error due to mismatch 2 receivers.

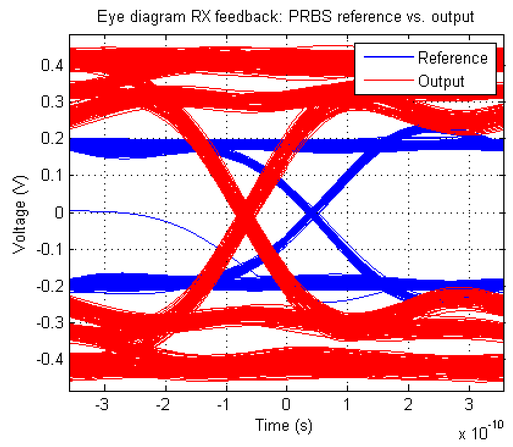


Figure 2: Eye diagram output LVDS/SLVS receiver with 200 mV amplitude, 800 mV common mode level and 2.56 Gbps, $2^7 - 1$ sequence PRBS input signal.

Trise / Tfall	250 ps
Crossing voltage	630 mV
Propagation delay asymmetry	6.25 ps
σ_{RMS}	3 ps
Power	500 µW

Table 1: Measurement results LVDS receiver

Mismatch compensation

- Altering duty cycle CLK input

→ 36 ps tuning range

- Initial error compensated at duty cycle of 55 %

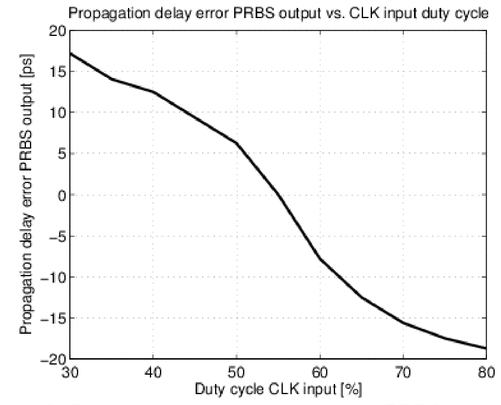


Figure 3: Propagation delay error of the PRBS output signal vs. the duty cycle of the CLK input signal

Radiation simulations: 500 Mrad (a)

	With compensation	Without compensation
Propagation delay	17.8 ns	17.9 ns
Propagation delay asymmetry	-1.2 ps	-11.6 ps
Difference vs. normal operation	+ 0.3 ps	+ 13.1 ps

→ 43 times less variation

Figure 4: Eye diagram output LVDS/SLVS receiver with 200 mV amplitude, 800 mV common mode level and 2.56 Gbps, $2^7 - 1$ sequence PRBS input: a) Normal vs. irradiated output signal with compensation. b) Normal vs. irradiated output signal without compensation.

(a) The radiation models have been made available by CPPM (Centre de Physique des Particules de Marseille) through the CERN RD53 collaboration.