A 4-Channel Parallel 56 Gb/s CMOS Optical Receiver for VCSEL-Based Optical Links

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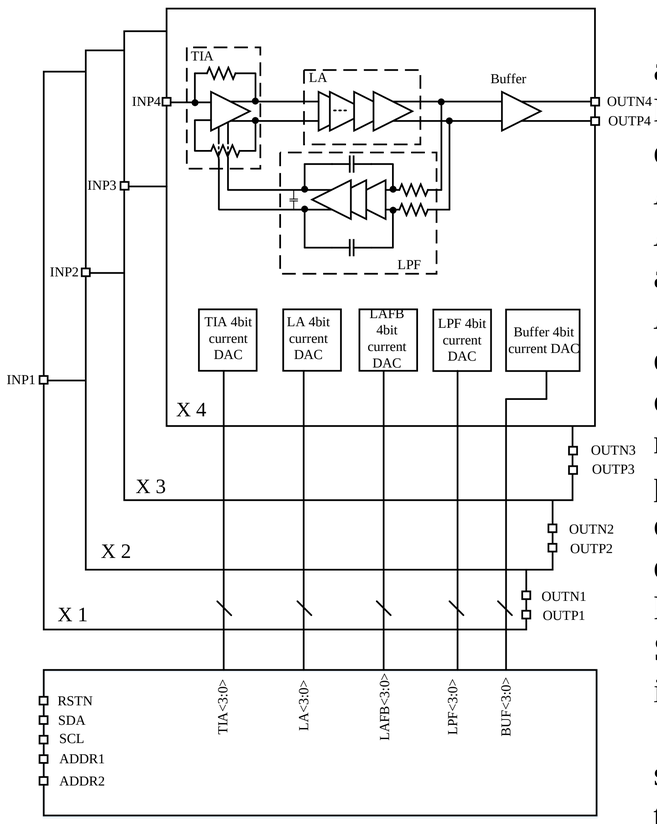
Abstract

A 4-channel 14 Gb/s CMOS optical receiver for VCSEL-based optical links is presented. The receiver has been manufactured in a 65 nm CMOS process. Simulation results under extracted layout parasitics and a model of a wire-bonded photo diode demonstrate the receiver has a bandwidth of 10.2 GHz, an input sensitivity of better than 20 μA_{pp}, an input-referred noise of 2.3 μA_{rms} and a differential output amplitude across an external 50 ohm load of larger than 400 mV_{pp}. The power consumption is 84 mW/channel for a power supply of 1.2 V.

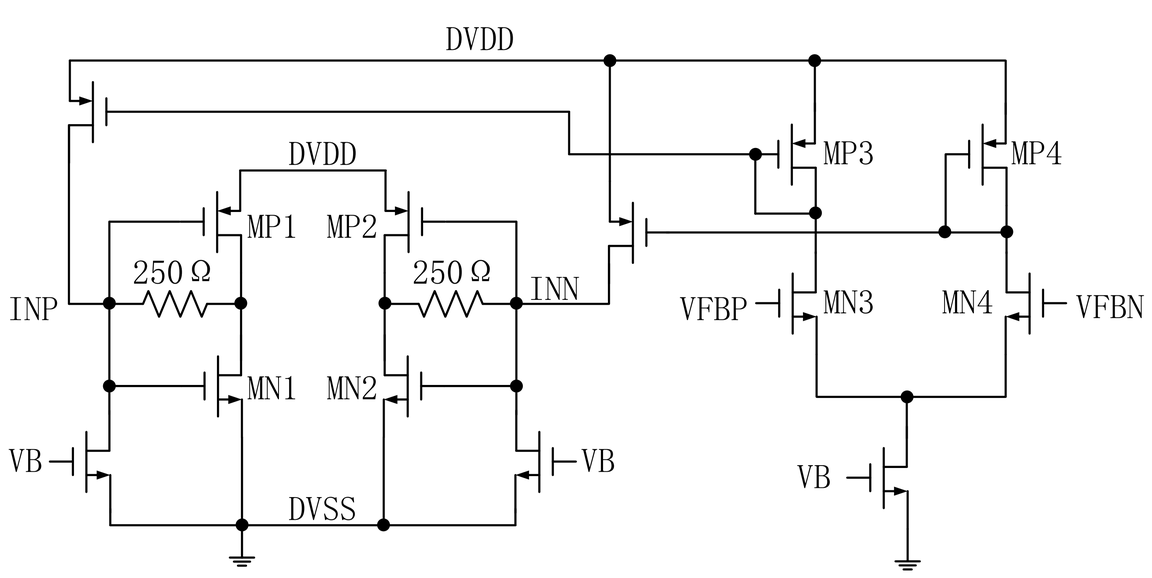
The system-level block diagram



The receiver is a four-channel array, each channel is up to 14 Gbps. Each channel consists of a pseudo-differential Transimpedance Amplifier (TIA), a Limiting Amplifier (LA) with interleaving active feedback and an output buffer. A 250 μm pitch between channels is designed with the same as the off-chip photo diode array. The receiver modulation current is programmable through an I^2C controller. The I^2C controller is designed with Triple Modular Redundancy (TMR) to increase the Single Event Upset (SEU) effect immunity.

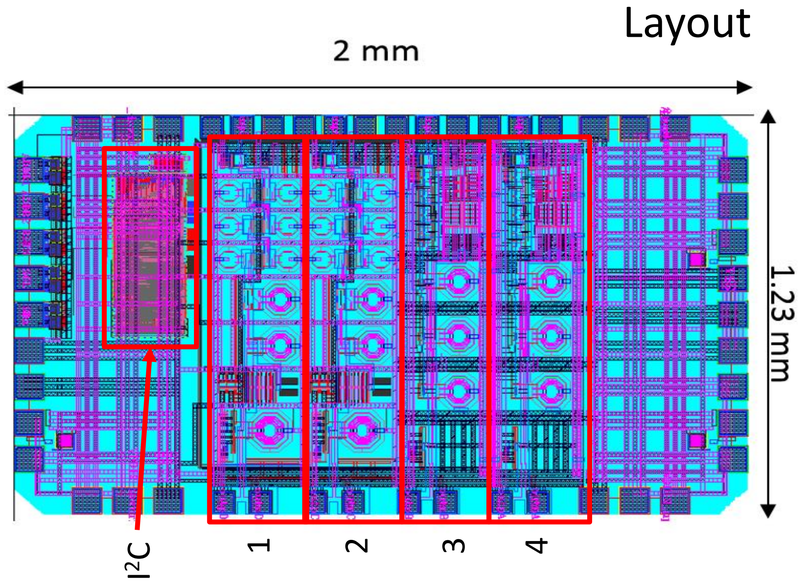
The LA of the first and the second channels are different from the one of the third and the fourth channels.

TIA



The TIA adopts a pseudo-differential structure to improve the power supply rejection ratio and common mode rejection ratio. A pair of CMOS inverters with resistive feedback, one active and one a replica, are used in the TIA. The simulation results show that the TIA gain is 200 ohm. With a photo diode DC coupled to the TIA, a 2.47 μA_{rms} input-referred noise and a 25 GHz bandwidth is measured in the post-layout simulations. The power consumption of the TIA is around 7.2 mW for a power supply of 1.2 V.

Layout

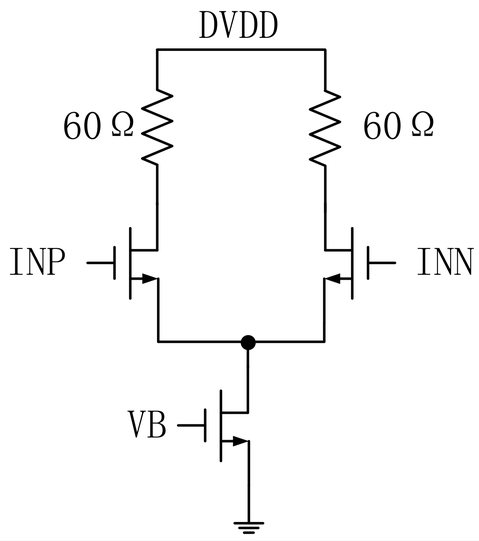


9 inductors are used in channel 1 and channel 2, respectively.

3 inductors are used in channel 3 and channel 4, respectively.

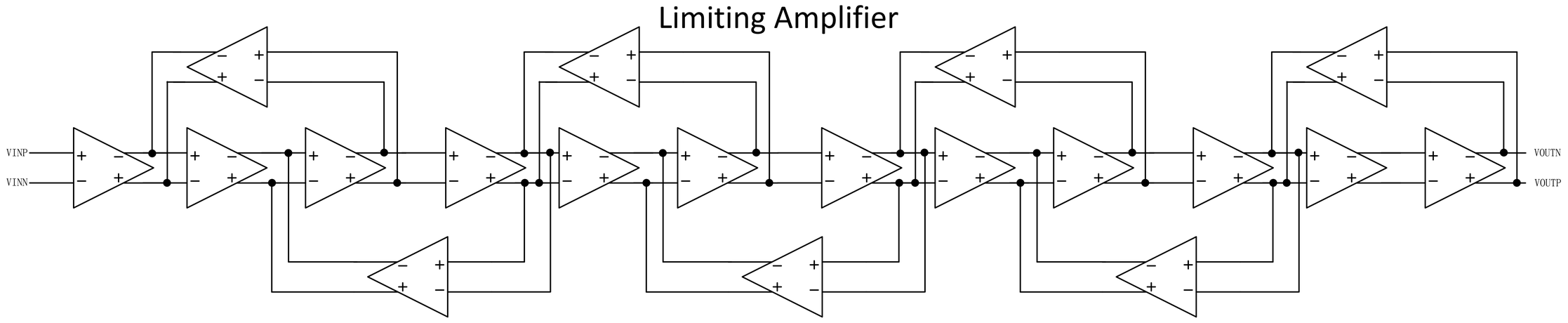
Two ground PADs are inserted between adjacent channels in order to reduce the crosstalk from the adjacent input signal bonding wires.

Output Buffer



The output buffer driving off-chip transmission line is a differential amplifier with a load resistance of 60 ohm. The bandwidth of the output buffer is 17 GHz with a power consumption of 14.4 mW for a power supply of 1.2 V.

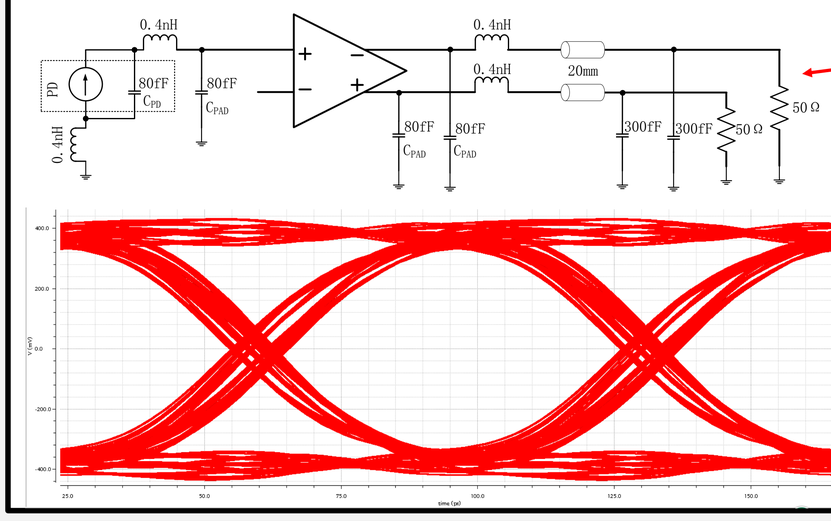
Limiting Amplifier



The LA is a 12-stage fully differential amplifier. Interleaving active-feedback structure is adopted in the LA to extend the bandwidth for each stage. The shunt inductive peaking technique is used to extend bandwidth in the last three-stage differential amplifiers of LA at the expense of area. The simulation demonstrates that the LA has a gain of 51 dB and a bandwidth of 13.3 GHz. The LA consumes 57 mW in total for a power supply of 1.2 V.

Simulation results

Setup: 14-Gbps PhotoDiode (PD) model, Input single-end current peak-to-peak 20 μApp 14-Gbps PRBS-7 signals, using channel 3 for the post-layout simulations.



Performances:

1. DJ: 9.5ps
2. RJ: 0.82ps
3. TJ: 20.98ps
4. max Vertical opening:661.7mV
5. max horizontal opening:60.96ps
6. rising time (20%~80%):36.82ps

Conclusions

The 4-channel parallel 56 Gbit/s optical receiver for VCSEL-based optical links has been manufactured in a 65 nm CMOS process in April 2017. The dimension of the whole chip is 1.23 mm × 2 mm. The simulation demonstrates that the receiver has a bandwidth of 10.2 GHz, an input sensitivity of better than 20 μA_{pp}, an input-referred noise of 2.3 μA_{rms} and a differential output amplitude across an external 50 ohm load of larger than 400 mV_{pp}, and consumes 84 mW/channel for a power supply of 1.2 V. The receiver is just under the test and we will get the results soon.

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