Development of A 3.2 Gbps Serial Link Transmitter for CMOS Pixel Sensors

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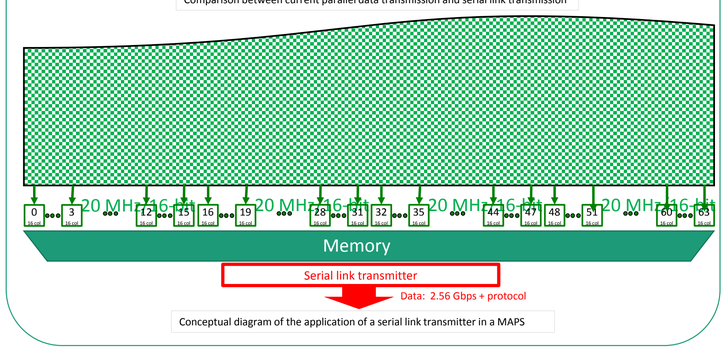
1. Motivation

- CMOS monolithic active pixel sensors(MAPS) for future subatomic physics experiments require integration of high-speed serial data link due to
  - Increasing hit-density
  - Low material budget
- We developed a 3.2 Gbps serial link transmitter for MAPS application

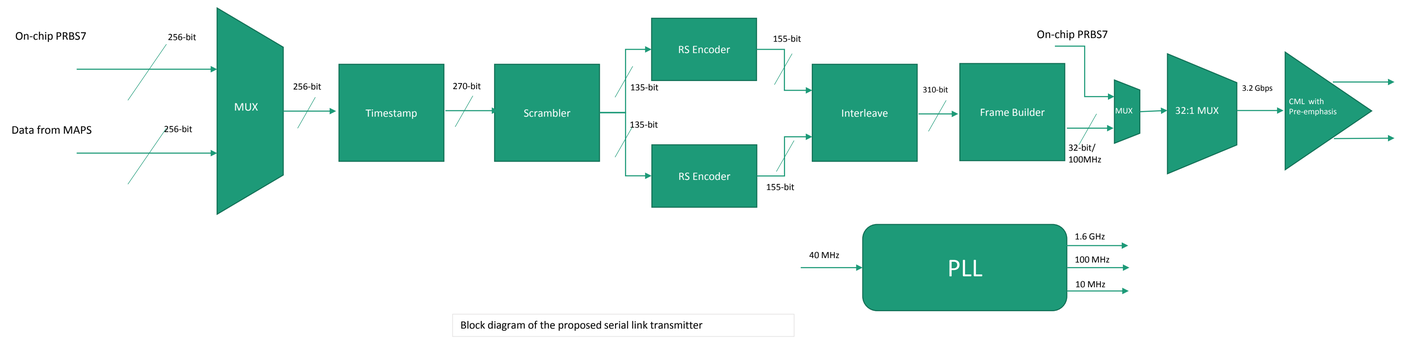
	Current Parallel Data Transmission(8 X 320 MBps, LVDS)	Serial Data Transmission
Cables	18 (16 of them for data and other 2 for clock)	2
Clock Skew	Yes	No
Error Correction	No error correction	Up to 20-bit in a frame

Comparison between current parallel data transmission and serial link transmission



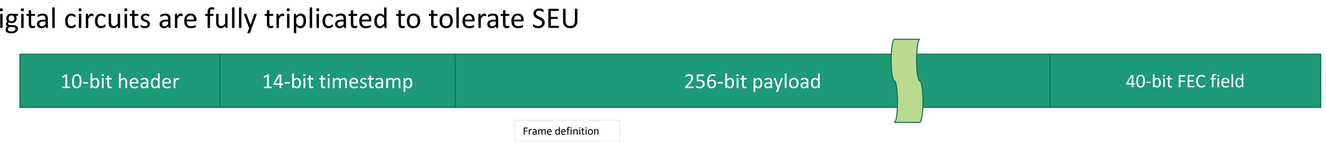
Conceptual diagram of the application of a serial link transmitter in a MAPS

2.Architecture



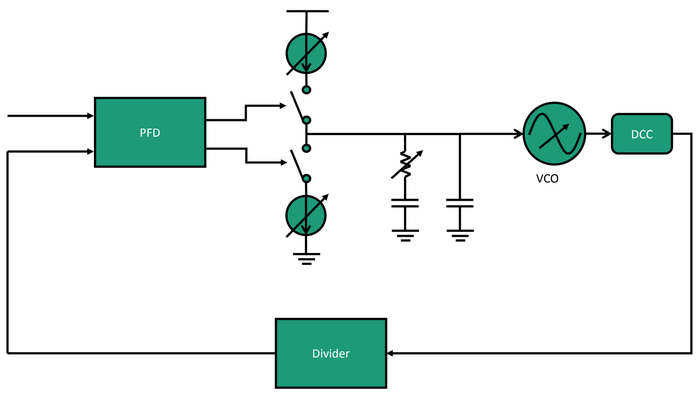
Block diagram of the proposed serial link transmitter

- 256-bit raw data at 10 MHz
- 14-bit timestamp
- Scrambler defined by polynomial $x^{58}+x^{39}+1$
- Interleaved Reed-Solomon (31,27) FEC encoder, correct burst bits up to 20-bit
- Digital circuits are fully triplicated to tolerate SEU
- Half-rate serialization scheme
- 1.6 GHz clock generated with duty-cycle correction
- 32:1 multiplexer with 5-stage binary-tree structure
- CML driver with 3-tap pre-emphasis
- On-chip PRBS-7 for testability

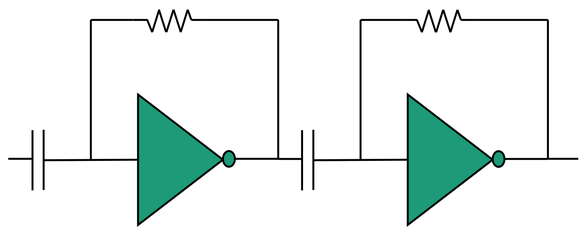


Frame definition

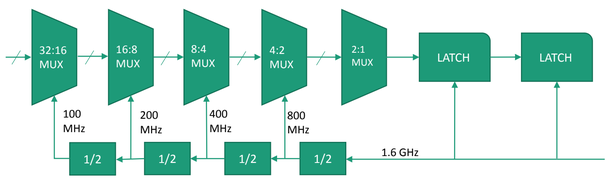
3. The PLL and the serializer



Block diagram of the PLL



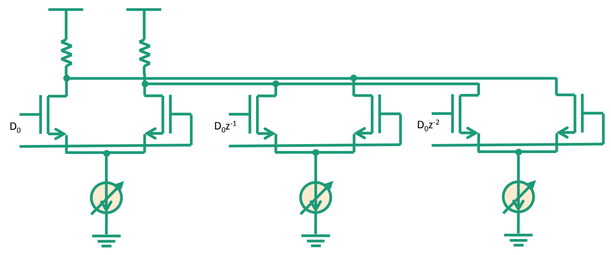
Simplified schematic of the duty-cycle correction circuit



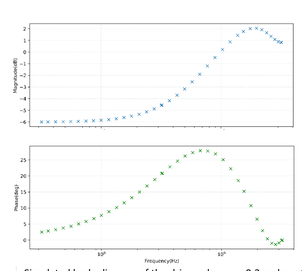
5-stage binary tree serializer

- Charge-pump PLL for clock multiplying by a factor of 40
- Loop bandwidth is programmable to ease in-band noise and out-band noise trade-off
- 4-stage ring voltage-controlled oscillator covers frequency ranging from 0.8 GHz to 2.4 GHz
- Duty-cycle correction circuit minimizes duty-cycle distortion(DCD)
- The divider is fully triplicated to tolerate SEU
- 5-stage binary-tree structure based serializer

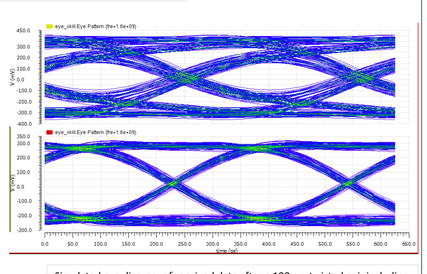
4. The Pre-emphasis



Simplified schematic of the CML driver with pre-emphasis



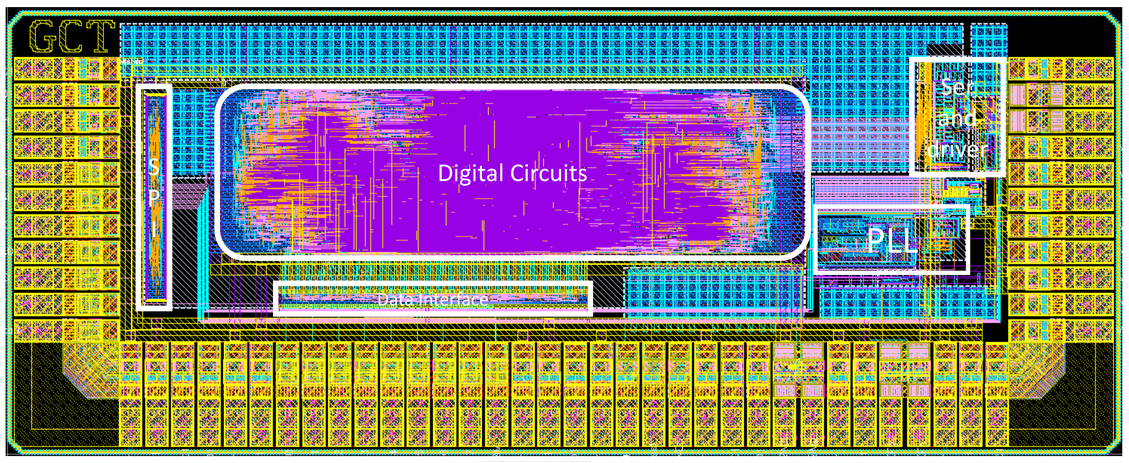
Simulated bode diagram of the driver when a_0=-0.3 and a_1=-0.2. A 10 dB peaking could be obtained



Simulated eye diagram of received data after a 100 cm twisted pair including parasitic devices: pre-emphasis on(upper), pre-emphasis off(lower)

- Pre-emphasis was implemented in the driver because low mass cables are preferred in the system
- Output CML driver realizes programmable 3-tap pre-emphasis
  - Z-domain transfer function: $Y(z^{-1}) = I_o(1 + a_0z^{-1} + a_1z^{-2})$
- 2 delayed copies of data are generated by the serializer

4. Results Summary



Layout of the chip

Technology	Towerjazz 0.18 µm CIS CMOS Process
Core Area	2360 µm X 760 µm
Supply Voltage	1.8 V for both IO and core
Data Rate	3.2 Gbps
Reference Clock	40 MHz
Differential Output Swing	Maximum 800 mVpp
Encoding	RS (31, 27)
Frame length, efficiency	320-bit, 84.375%(256-bit data and, 14-bit timestamp)
Power consumption	173.9 mW in total • PLL: 39.0 mW, • Clock distribution: 6.8 mW, • Serializer: 20.7 mW, • Driver: 37.4 mW • Digital circuits: 69.8 mW

Summary of the transmitter. power consumption is from simulation

5. Conclusion and outlook

We developed a serial link transmitter for CMOS pixel sensors application in a 0.18 µm CMOS Technology. The transmitter includes a Reed-Solomon encoder, a PLL, a serializer and a Current Mode Logic (CML) driver with pre-emphasis. Functionalities of the transmitter is verified by simulation, consuming 174 mW from a 1.8 V power supply.

This is the first time that a multi-Gbps serial link transmitter is developed as a high-reliability, low-mass, low-power consumption data transmission solution for MAPS. The prototype was submitted standalone and measurement will be carried out in November. We aim to integrate it into a CMOS sensor chip later.

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