Contribution ID: **110** Type: **Poster**

A 3.2 Gbps Serial Link Transmitter for CMOS Pixel Sensors in 0.18 µm CMOS Technology

Tuesday 12 September 2017 17:45 (15 minutes)

We present a serial link transmitter designed for CMOS pixel sensors in a 0.18 µm CMOS Technology. The transmitter includes a digital interface block with Reed-Solomon encoder, a Phase-Locked Loop (PLL), a serializer and a Current Mode Logic (CML) driver with pre-emphasis. Functionalities of the transmitter is verified by simulation, consuming 174 mW from a 1.8 V power supply. The transmitter aims to be integrated into a CMOS sensor chip, but this first prototype will be fabricated standalone in this May. We will report the measurement results in the final paper.

Summary

Numerous future subatomic physics experiments demand CMOS pixel sensors with high-speed serial data links due to the increasing hit density, low material budget requirements. A serial data link meets requirement of this application due to its saving cables/connectors and high reliability in contrast to a parallel data link. We present a serial link transmitter designed for CMOS pixel sensors in a 0.18 µm CMOS Technology. The transmitter encodes the received pixel data with Reed-Solomon correction algorithm and send data in serial at 3.2 Gbps. The transmitter includes a PLL for clock generation, a digital interface block with Reed-Solomon encoder, a serializer and a CML driver with pre-emphasis. The radiation immunity is considered in the whole design.

The PLL generates a 1.6 GHz clock from a 40 MHz reference clock. A ring Voltage-Controlled Oscillator (VCO) is employed because of low power consumption. The VCO consists of four delay cells with positive feedback to gain fast slewing. The charge pump current and he loop filter resistor is programmable to minimized the jitter performance. Because the half-rate serializer structure is sensitive to the duty cycle of clock signal, a duty-cycle correction circuit is used to alleviate Duty-Cycle Distortion (DCD). The clock divider in the PLL loop is triplicated to resist SEU.

The digital interface block encodes the user data into 320-bit data frame in which there are 10-bit frame head, 256-bit pixel data, 14-bit timestamp and 40-bit overhead. The 256-bit raw data is received at 10 MHz from a CMOS sensor. In this prototype, we generate the 256-bit raw data through a pseudorandom binary sequence (PRBS) to emulate sensor data. The data with timestamp is scrambled and then encoded with Reed-Solomon algorithm. There are up to 20 consecutive bits could be corrected in a frame, benefiting from this RS(31,27) encoding in our scheme, which is suitable for burst errors in subatomic experiments. The penalty is a 40-bit overhead being added to the payload. The digital interface block delivers data with 32-bit width at frequency of 100 MHz to the serializer. The digital interface block is fully triplicated because that the feedbacks in the scrambler and the encoder are sensitive to errors induced by SEU.

The serializer is a 32:1 multiplexer with 5-stage binary-tree structure. Only the last stage is sensitive to duty-cycle error of the clock that is mitigated by the duty-cycle correction circuit. The serializer provides a complementary signal and its two copies of one and two clock period delay to the CML driver.

The CML driver realizes pre-emphasis with one main driver and two post-taps. The output swing and the tap coefficient is programmable. The maximum swing when all the pre-emphasis are off is 800 mV across two 50 Ω internal termination resistors.

The 3.2 Gbps serial link transmitter is designed in a 0.18 µm CMOS technology. The functionalities are verified

by simulation. The transmitter consumes 174 mW from a 1.8 V power supply. The prototype will be submitted in May. We expect to report the measurement results in the final paper.

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Session Classification: POSTER Session

Track Classification: ASIC