Karlsruhe Institute of Technology

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Institute for Data Processing and Electronics

Development of a Front-End ASIC for 1D Detectors with 12 MHz Frame-Rate

L. Rota **(lorenzo.rota@kit.edu)**, **M. Caselle (michele.caselle@kit.edu)**, A. Mozzanica, B. Schmitt, E. Bründermann, A.-S. Müller, M. Weber

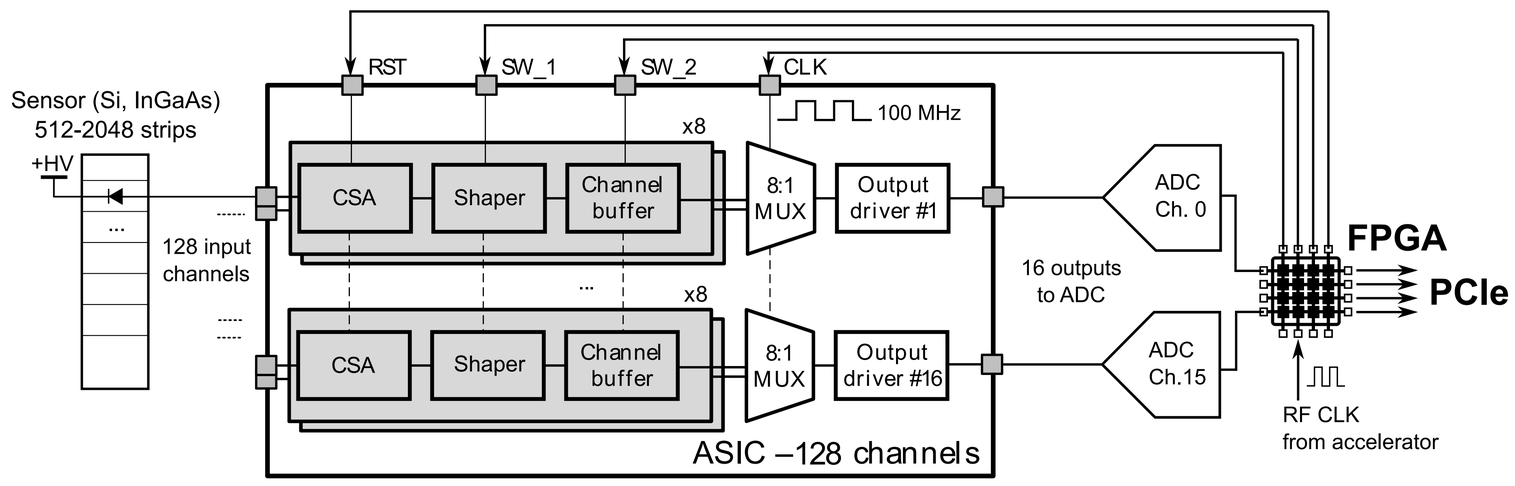
Motivation

Front-end ASIC for a 1D imaging detector with continuous acquisition and a large number of channels at MHz frame rates **KALYPSO** → **see poster E2 tomorrow!**

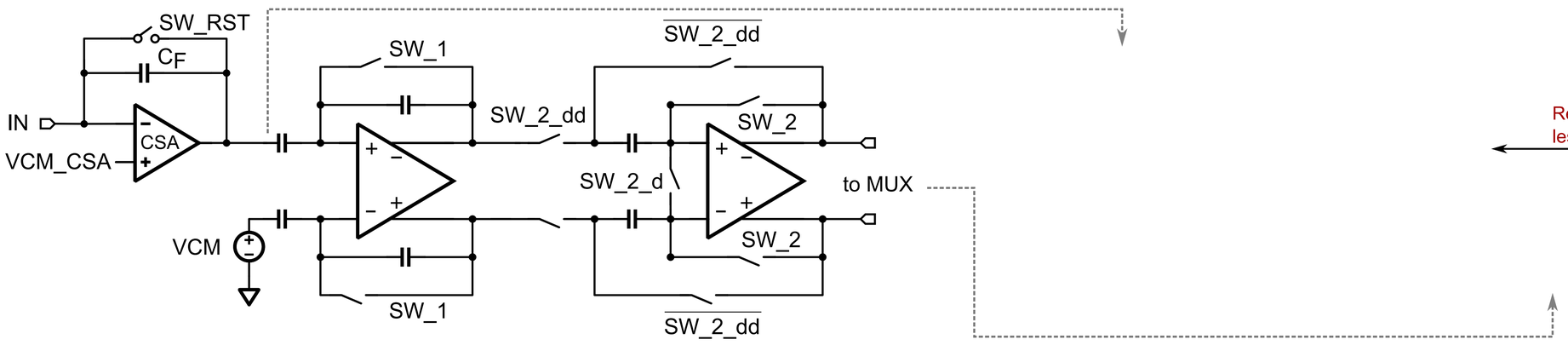
Architecture

Main specifications

- Technology: UMC 110 nm, 1.2 V
- Compatible with different microstrip sensors
  - Signal polarity: *p-in-n* or *n-in-p*
  - Detector capacitance: 0.5 - 5 pF
  - Semiconductor material: Si, InGaAs, *etc.*
- Frame-rate up to 10 Mfps
  - Continuous → 1.28 GS/s each chip
  - Channel buffer → *integrate-while-read* operation
- Noise < 500 e^- @ 1.3 pf
- Mounted on FPGA mezzanine card
  - High PSRR & CMRR → differential architecture

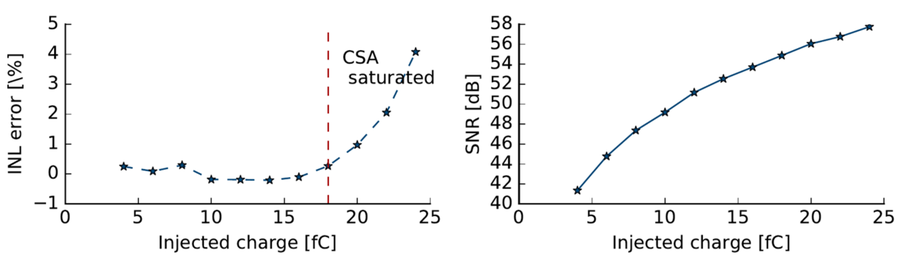


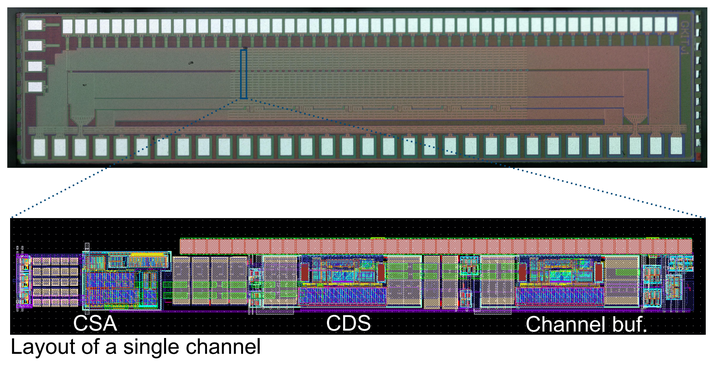
First prototype with 48 channels



Results

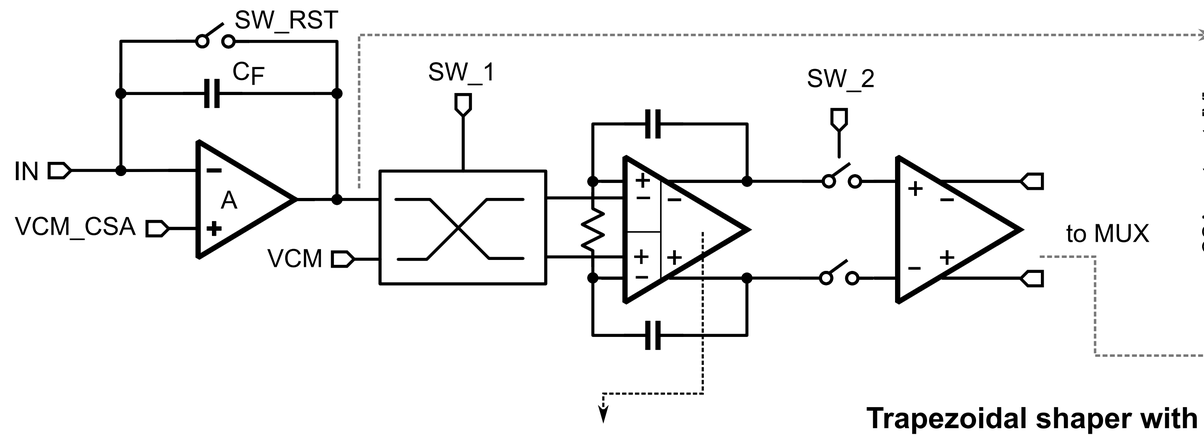
- Noise 217 e^- + 153 e^-/pF
- Integral nonlinearity (INL) < 0.5%
- Cross-talk < 0.2% (without sensor)
- Frame-rate: 12 MHz

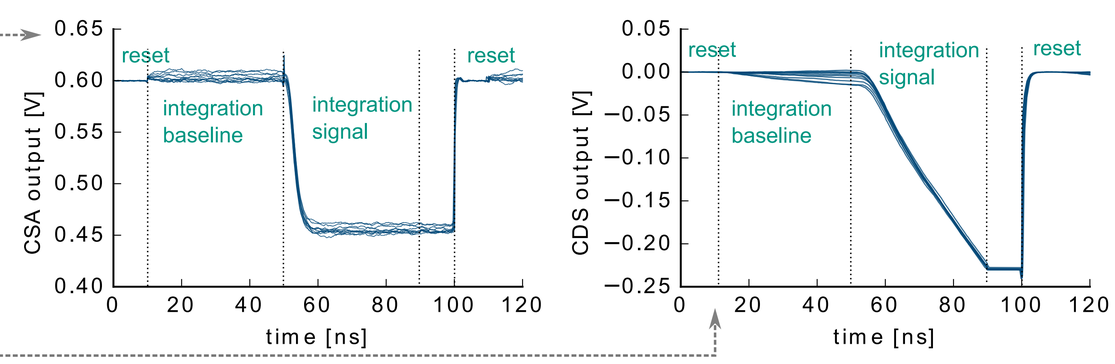




Layout of a single channel

Future work: improved noise performance





Trapezoidal shaper with Fully Differential Difference Amplifier (FDDA):

- Implement in a single stage *single-ended to differential* conversion + shaping
- Improve CDS filter to remove kT/C and low-frequency noise components
- Trapezoidal integration reduces white noise components
- No resistive load on CSA
  → source-follower output stage can be avoided
- No feedback path on VCM reference
  → reduce crosstalk for ASICs with many channels

Shaping time can be tuned according to the specific application:

- Detector capacitance of Si microstrip
- Required frame rate