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Development of a Front-End ASIC for 1D Detectors with 12 MHz Frame-Rate

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We present a front-end readout ASIC developed for a new family of ultra-fast 1D detectors. The ASIC is designed in 110 nm CMOS technology and is compatible with different semiconductor sensors (Si or InGaAs) and geometries. The chip contains up to 128 channels, each consisting of a Charge-sensitive Amplifier, a fully-differential shaping stage and an high-speed output buffer. A frame-rate of 12 MHz at full occupancy has been obtained with the first prototype. We also discuss a novel circuital solution to implement tunable time-variant trapezoidal shaping based on a Fully-Differential Difference Amplifier, to improve noise performance at high frame-rates.

Summary

A fully custom ASIC has been developed for a new generation of 1D detectors to be used for beam diagnostics at accelerators . The main requirements are a frame-rate in the MHz range with full occupancy, high-linearity and low-noise performance. Moreover, since the chip will be integrated on a detector card together with high-speed digital and RF circuits, high rejection of common-mode and power-supply noise are mandatory. Finally, the chip must be able to process signals of both polarities with a variable detector capacitance (from 500 fF to 5 pF), in order to be compatible with different sensor technologies,.

The chip is designed in 110 nm CMOS technology from UMC. The final version of the chip will consists of up to 128 channels with 50 µm pitch, to match the geometry of the sensors. Each channel is based on a synchronous readout and consists of a Charge-Sensitive Amplifier (CSA), a noise-shaping stage and a channel buffer. The CSA amplifier is implemented as a differential folded-cascode OTA.
The noise-shaping stage performs Correlated-Double-Sampling (CDS) in order to reduce low-frequency noise and the kT/C noise introduced by the synchronous reset mechanism. In order to achieve high frame-rates, a sample-and-hold channel buffer is needed to allow "integrate-while-read"operation.

The output of each channel is connected through an analog multiplexer to a high-speed I/O buffer, which drives the external ADC with a settling time below 4 ns. To achieve high speed and low distortion with a 50 Ohm load, the output buffer has been designed with a two-stage class-AB OpAmp with cascode Miller compensation.

A first prototype based on a traditional CDS stage and with a limited number of channels has been submitted and characterized. With a power-supply voltage of 1.2 V and a power consumption of 1.7 mW/channel (including the 50 Ohm line-drivers), we have measured a gain of 37 mV/fC, a maximum frame-rate of 12 MHz and an ENC of 400 e- @ 1 pF at the maximum readout speed.

To improve the noise performance of the system, a novel time-variant noise-shaping stage has been designed. A novel circuital solution based on a Fully-Differential Difference Amplifier (FDDA) allows us to incorporate both noise-shaping and single-ended-to-differential conversion in a single stage, without loading the output of the CSA with a resistive load. With respect to the previous design based on a traditional CDS stage, simulations have shown a significant improvement in noise performance while maintaining the same power consumption. Moreover, the shaping time can be tuned according to the required frame-rate, therefore optimizing noise performance. An ENC of 140 e- @ 1 pF and a 10 MHz frame-rate has been estimated through Monte-Carlo simulations. The final version of the chip with the new noise-shaping stage will be submitted in summer 2017.

We will discuss the implementation and the characterization of the first prototype chip together with the improvements developed for the final version. In particular, we will describe the trapezoidal-shaper based on FDDA and compare it with other solutions present in the literature.

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