MATISSE: a low power front-end electronics for MAPS characterization

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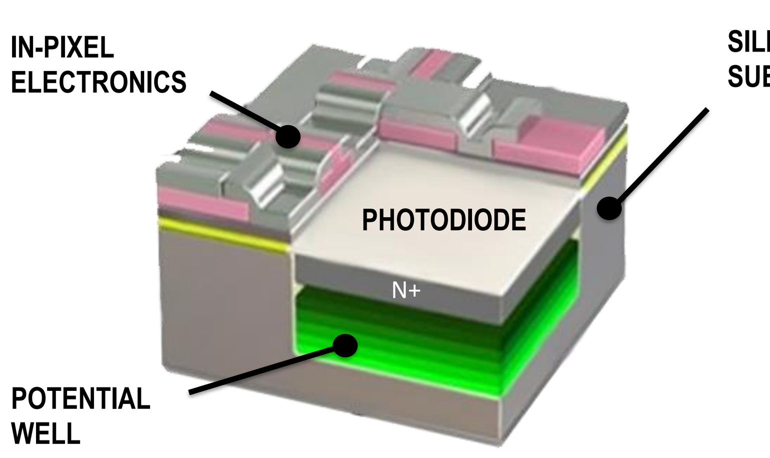
Abstract

- The future generation of **HEP experiments** must deal with unique requirements, encouraging the development of novel radiation silicon sensors technologies suitable for extreme radiation environments. In recent years **monolithic pixel sensors (MAPS)** are becoming increasingly attractive thanks to their good properties. Here are proposed the first results of a flexible front-end electronics developed into an R&D program of monolithic sensors.

Monolithic Sensors

Example of monolithic pixel



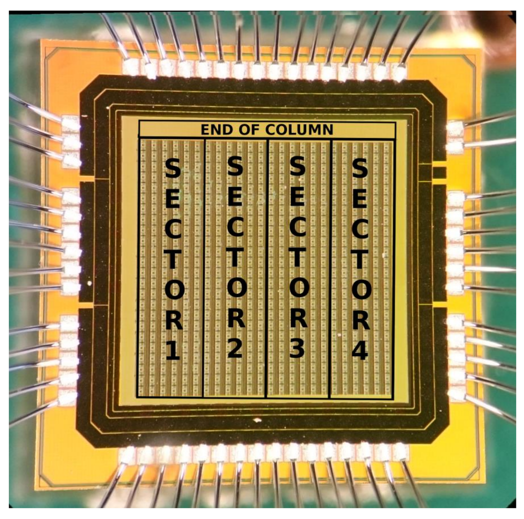
PROs
- Low material budget
- Cost
- High granularity
- No bump bonding required

CONs
- Low flexibility
- Small area for the electronics
- Sensor only partially depleted

The MATISSE ASIC

MATISSE = Monolithic AcTIve SenSor Electronics

- First prototype developed in 0.11 µm CMOS VLSI technology with a die area of 2×2 mm^2
- The chip has been received from the foundry in April 2017
- It consists of 24×24 pixel matrix organized in 4 independent sectors (6×24) and an End of Column logic (EoC)
- The analog data is sent off-chip through two independent data buses shared between the pixels of each sector

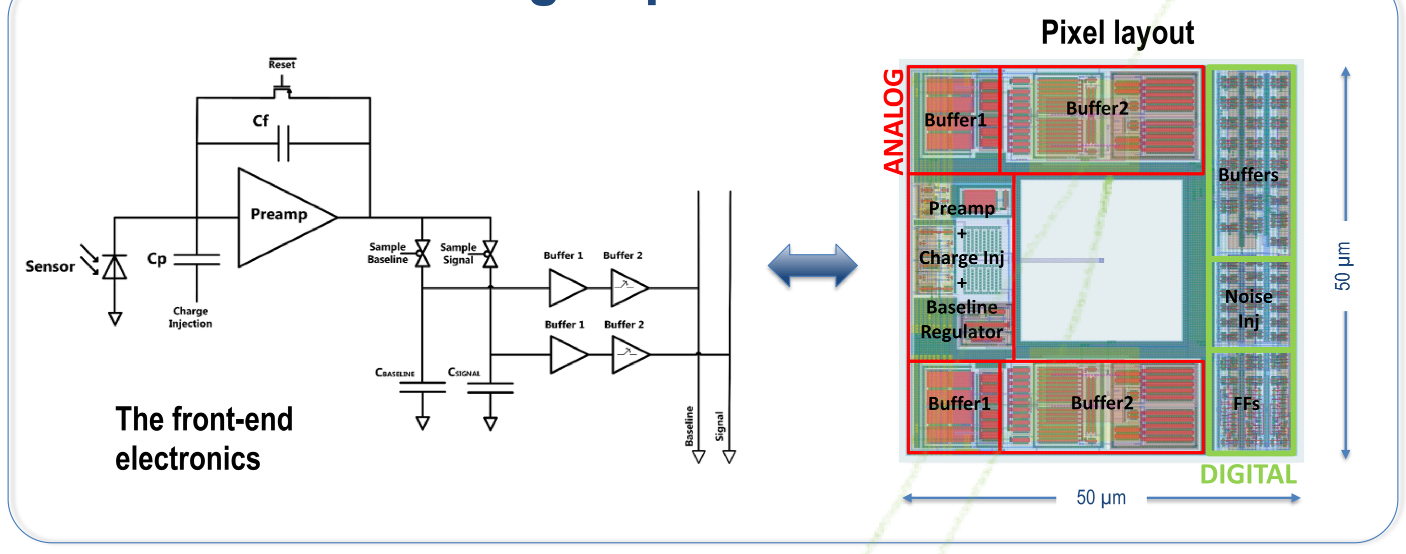


The pixel unit

Main parameters

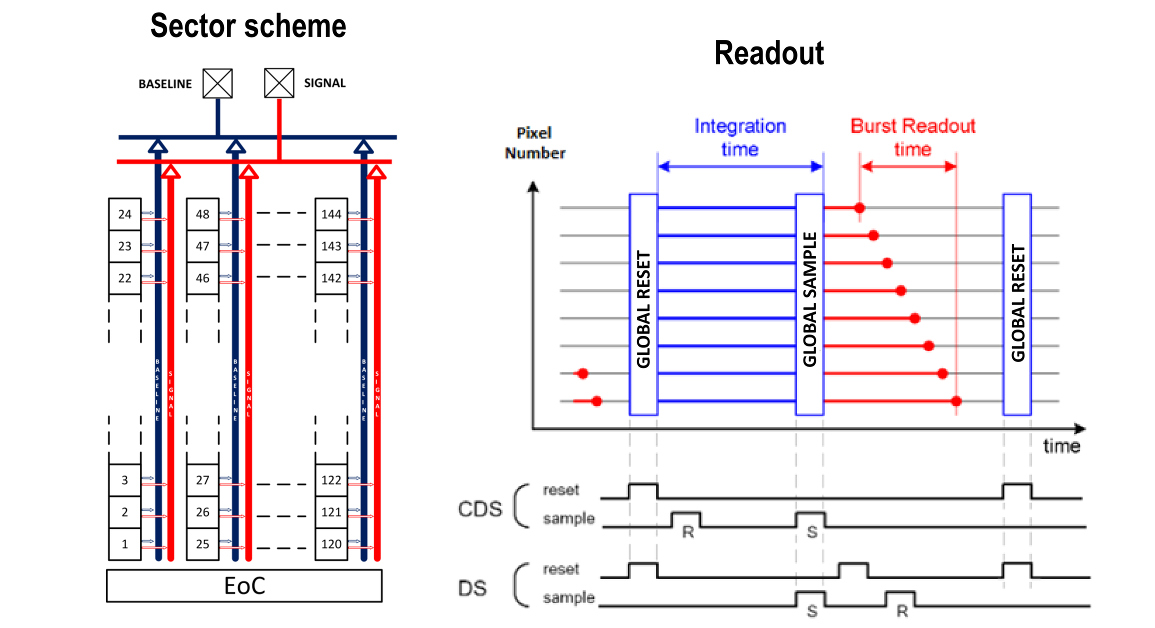
PARAMETER	VALUE
Analog Gain	~ 163 mV/fC (2.7 mV/100 e⁻)
Noise	~ 40 e⁻
Power consumption	Waiting: ~ 6 µW Transmission: ~ 370 µW
Sensor Cap	40 fF
Storage Caps	~ 70 fF (MIM CAPS)
Linearity range	400 mV – 950 mV
Readout speed	Up to 5 MHz
Other features	Internal Test Pulse Mask mode Baseline regulator
Shutter type	Snapshot shutter
Readout type	Correlated Double Sampling

The analog in-pixel electronics



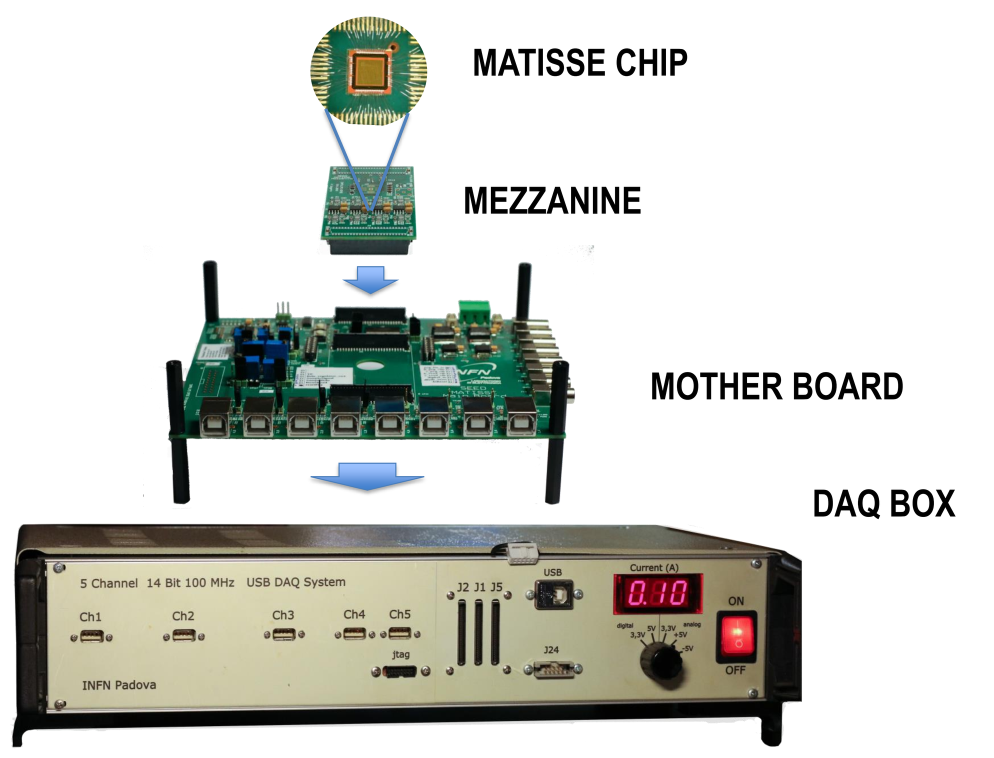
- Both NMOS and PMOS transistors are used
- The electronics fits an area of 30 µm × 30 µm
- Digital in-pixel logic manages:
  - The baseline voltage
  - The mask mode
  - The test pulse injection
  - The regeneration of digital signals

The readout operation



- MATISSE supports snapshot shutter operation
- The integration time can be as short as 100 ns
- The logic sequentially addresses the pixels of the sector
- The four sectors are readout in parallel
- Two analog outputs are sent off-chip

The full readout chain



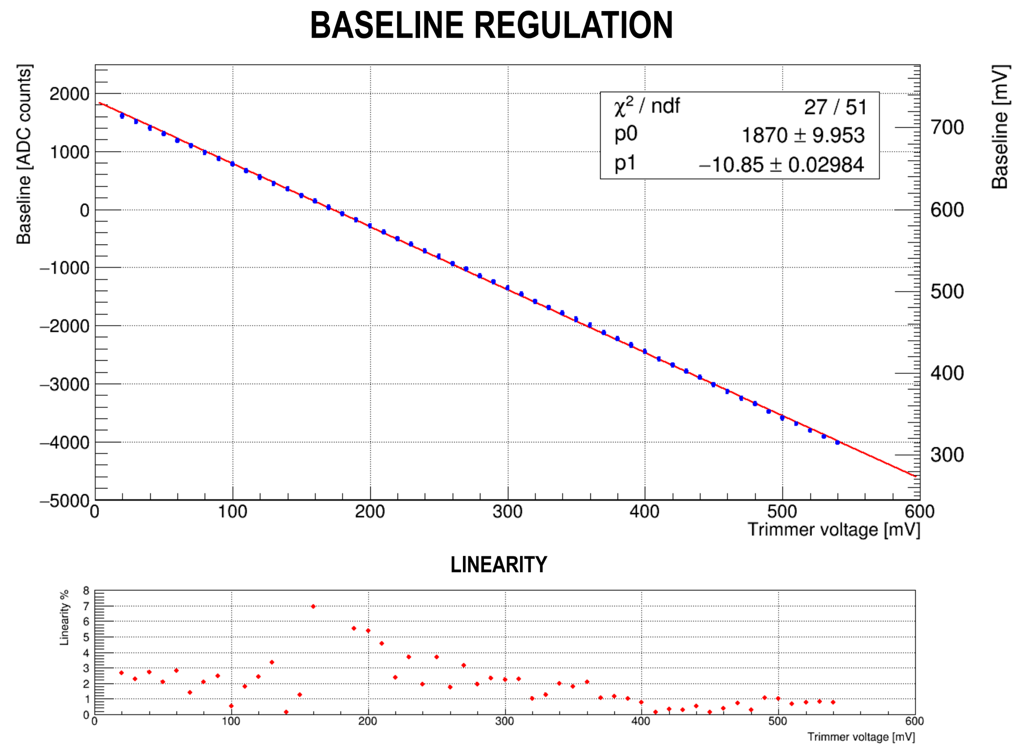
- ASIC and mezzanine connected through wire bonding
- The mother board contains most part of the electronics
- The DAQ box is based on:
  - custom analog board 5 CHs, 14 bit, 100 MHz
  - commercial FPGA board

NOISE IN THE FULL CHAIN

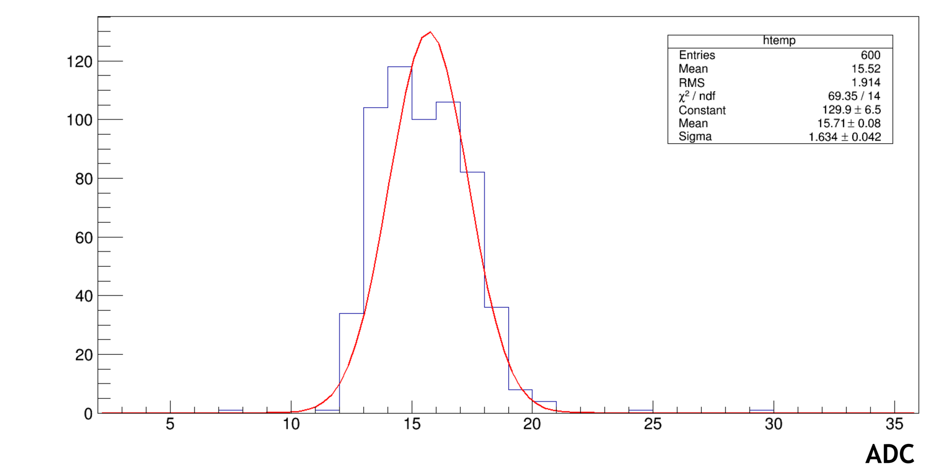
DEVICE	NOISE [ADC]	NOISE [mV]
DAQ	0.2	0.02
DAQ + MB	0.2	0.02
DAQ + MB + MEZZ	1.6	0.11
DAQ + MB + MEZZ + ASIC	15	1

Experimental results

BASELINE REGULATION

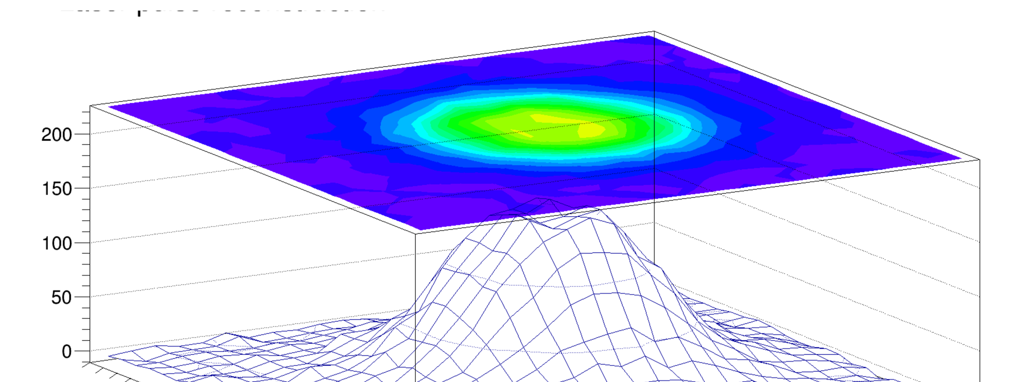


NOISE DISTRIBUTION

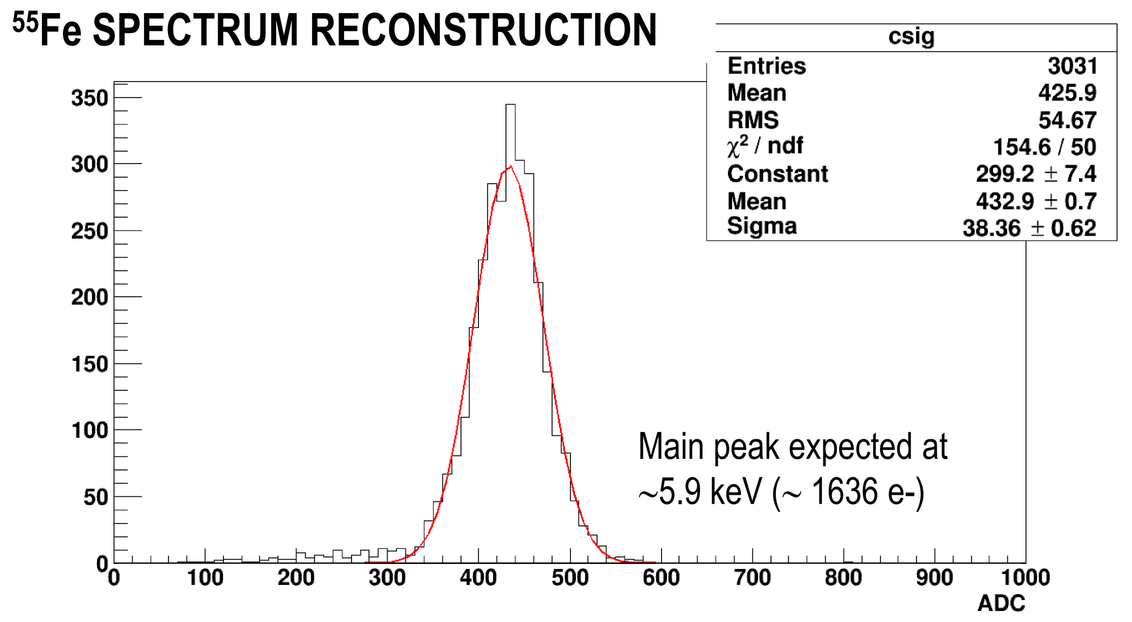


- The baseline can be tuned as desired up to 300 mV with a good linearity in the full range
- The measured noise is 15 ADC counts (1mV). It is measured as the fluctuation of the baseline of each pixel after the regulation

LASER PULSE RECONSTRUCTION



^{55}Fe SPECTRUM RECONSTRUCTION



- The analog input sent to the DAQ box allows the reconstruction of laser pulses
- The full system has been used also with an active source (^{55}Fe). The reconstructed spectrum allows to clearly distinguish the main peak expected at ~ 5.9 keV

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