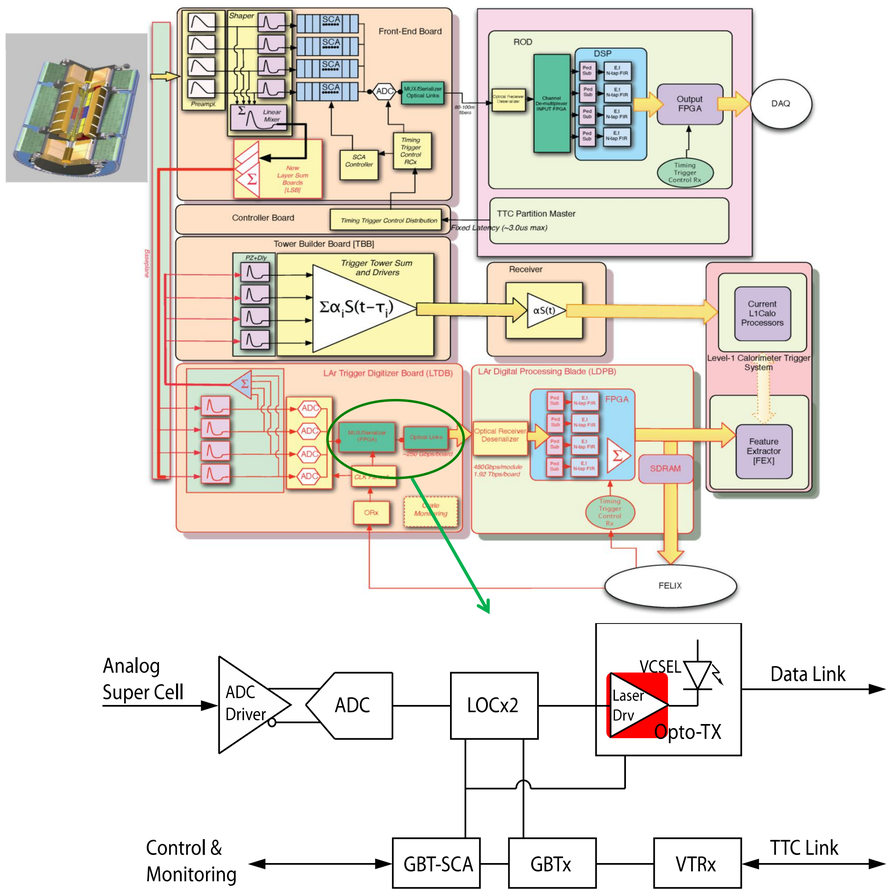
Developments of Two High-speed Dual-channel VCSEL Driver ASIC

Wei Zhou,[a,b] Xiao Le,[a] Di Guo,[b] Quan Sun,[b] Datao Gong,[b] Guangming Huang,[a] Chonghan Liu,[b] Tiankuan Liu,[b] Xiangming Sun,[a] Jingbo Ye,[b]
[a] *Department of Physics, Central China Normal University,Wuhan, Hubei 430079, P.R. China*
[b] *Department of Physics, Southern Methodist University, Dallas, TX 75275, USA*
sphy2007@126.com, dgong@mail.smu.edu



a) ATLAS LAr calorimeter readout and the LOCId chip in the optical readout system

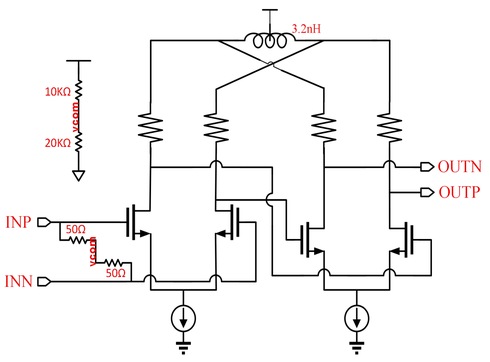
Introduction

LOCId-130 is a 5-Gbps dual-channel VCSEL driver ASIC designed in a commercial 130-nm CMOS process. LOCId-130 is designed to be a backup of LOCId that is pin-to-pin compatible. LOCId, based on a 0.25-μm CMOS process, is the baseline design for the Phase-I upgrade of the ATLAS Liquid Argon Calorimeter. The power consumption of LOCId is 220 mW. Benefiting from the 1.5 V power supply, the power consumption of LOCId-130 is 112 mW.

LOCId-65 is a 14-Gbps dual-channel VCSEL driver ASIC designed in a commercial 65-nm CMOS technologies. LOCId-65 is also pin-to-pin compatible to LOCId. LOCId-65 was submitted for fabrication on May 20th 2017. We expect to start the evaluation of this ASIC in lab and radiation environment in October to December of 2017. Here we present results from the post-layout simulation. The power consumption of LOCId-65 is 116 mW in typical case.

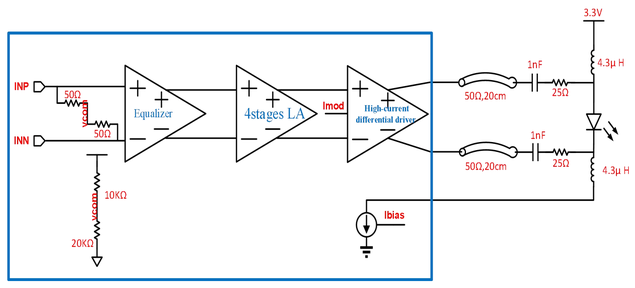
LOCId-130 Design

The analog core of LOCId-130 has two parts:
a limiting amplifier (LA) and a high-current differential driver. The minimum input signal is assumed to be 200 mV_{P-P}. The output is 8-mA modulation current CML. At the output both modulation and bias currents are programmable via I²C.

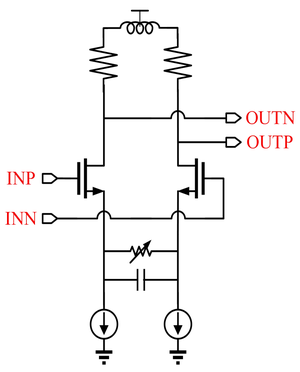


a) The structure of LA

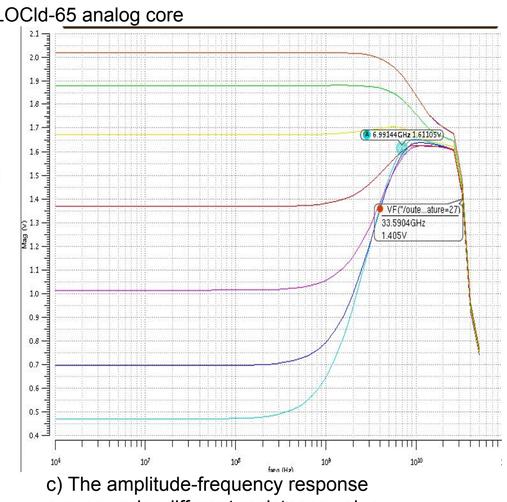
The LA adopts a two-stage differential amplifier with a 3.2-nH peaking inductor shared between these two stages, boosting the bandwidth to 3.5 GHz. The LA gain is 14 dB, amplifying input signal from 200 mV_{P-P} to 1 V_{P-P}.



a) The diagram of LOCId-65 analog core



b) The structure of equalizer

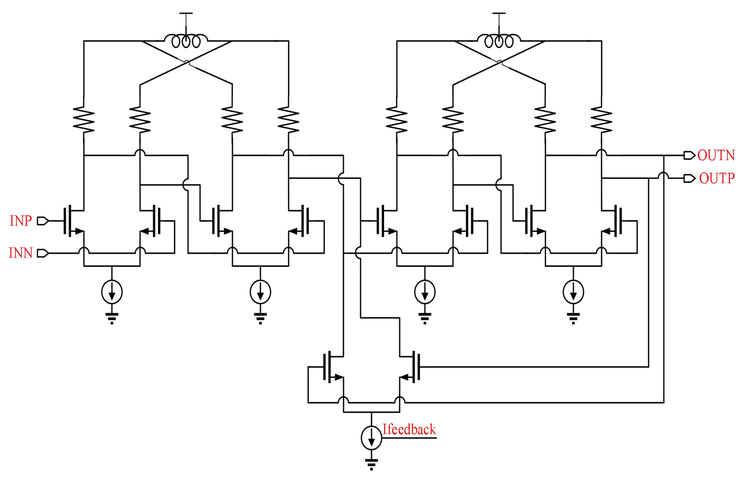


c) The amplitude-frequency response curves under different resistance value settings

Equalizer in LOCId-65 compensates the high-frequency signal loss due to the transmission line and the ESD diode. Fig c) shows the amplitude-frequency response curves under the different resistances.

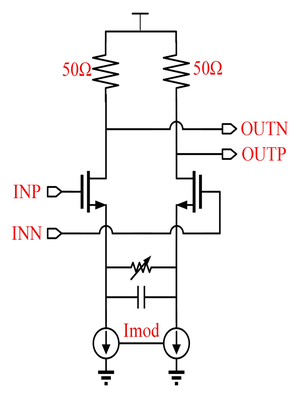
LOCId-65 Design

The input signal swing of LOCId-65 is expected to be 100 mV_{P-P} and the data rate is considered to be 14 Gpbs. Therefore, several techniques are used to boost the gain and the bandwidth. LOCId-65 consists of an equalizer, a four-stage LA and a high-current differential driver with pre-emphasis. The LA gain and the bandwidth are tunable via I²C.



d) The structure of four-stages LA

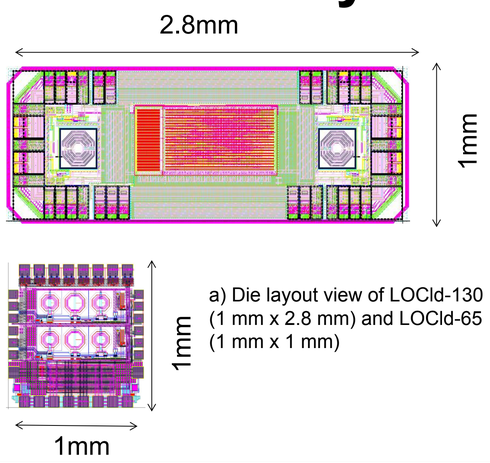
We use a four pre-drive stages to amplify signal amplitude to 800 mV_{P-P}. Every two-stage amplifier shares a peaking inductor to save the chip area. A current adjustable active feedback cell is used to adjust the gain and bandwidth of LA.



e) The structure of high-current differential driver

The output driver has a pre-emphasis option to improve the output signal bandwidth above 10 GHz in all process corners.

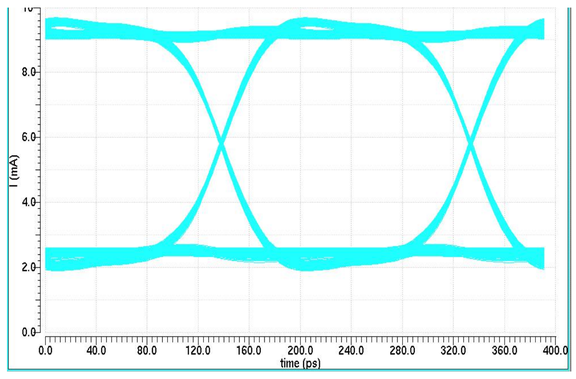
LOCId-130 and LOCId-65 layout



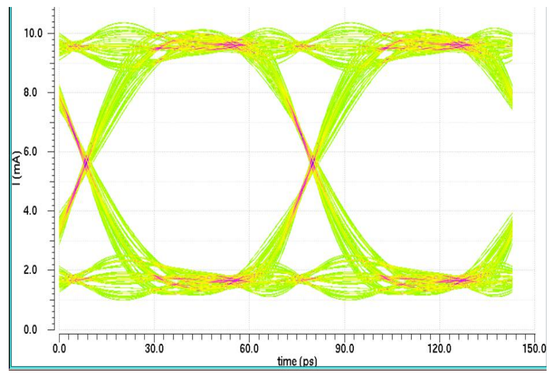
a) Die layout view of LOCId-130 (1 mm x 2.8 mm) and LOCId-65 (1 mm x 1 mm)

Compare LOCId-130 and LOCId-65

	LOCId-130	LOCId-65
Number of channels	2 channels	2 channels
Minimum Input signal	200 mV_{P-P}	100 mV_{P-P}
operates data rate	5 Gbps	14 Gbps
Equalizer	No	Yes
Power consumption	112 mW	116 mW
Control circuit	I²C	I²C
Die size	1 mm x 2.8 mm	1 mm x 1 mm
Package	QFN-40	QFN-40
Status	Plan to submit	Submitted



a) Typical Eye diagrams of laser current when LOCId-130 operates at 5 Gpbs



b) Typical Eye diagrams of laser current when LOCId-65 operates at 14 Gpbs

Acknowledgments

- This work is supported by SMU's Dedman College Dean's Research Council Grant, the US Department of Energy Grant DE-FG02-04ER1299 and by the China Scholarship Council (CSC).
- The authors are grateful to Paulo Moreira, Syzmon Kulis and Sandro Bonacini from CERN for discussions and guidance.

References

1. ATLAS collaboration, ATLAS liquid argon calorimeter Phase-I upgrade technical design report, CERN-LHCC-2013-017, ATLAS-TDR-022 (2013).
2. T. Zhang et al, "A 10 Gb/s Laser Driver in 130 nm CMOS Technology for High-energy Physics Applications," Proceedings of Topical Workshop on Electronics for Particle Physics 2014.
3. X. Li et al. 8-Gbps-per-channel radiation-tolerant VCSEL drivers for the LHC detector upgrade[J]. Journal of Instrumentation, 2015, 10(02): C02017.

TWEPP 2017 - Topical Workshop on Electronics for Particle Physics
September 11-15, 2017, UC SANTA CRUZ , USA