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Two High-Speed Dual-Channel VCSEL Driver

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We present two designs of a dual-channel VCSEL driver ASIC, named LOClD130 and LOClD65, aiming for the upgrade of ATLAS Liquid Argon Calorimeter. Each channel of the driver operates at 5 Gbps or 10 Gbps respectively. They are implemented in commercial 130 nm and 65 nm CMOS technologies. In typical case the 5 Gbps driver dissipates 56 mW/channel (VCSEL included) and the 10 Gbps 58 mW/channel. Both designs will be prototyped this summer.

Summary

Based on years of R&D, wafers of the dual-channel VCSEL driver, LOClD, implemented in a commercial 250 nm Silicon-on-Sapphire CMOS technology are produced. LOClD is the baseline choice for ATLAS Liquid-Argon-Calorimeter trigger upgrade. We design LOClD130 as a drop-in backup to LOClD, benefiting from the 1.5 V 130 nm technology to save power. We develop LOClD65 using the same 65 nm technology with which lpGBT is being developed. lpGBT is the serializer-deserializer (SerDEs) ASIC developed chiefly for upgrades of the HL-LHC. The serializer operates at 5 or 10 Gbps. While the predecessor of lpGBT, the GBTx SerDes has a matching optical transceiver (VTRx) developed through the Versatile Link common project, the optical module being investigated in VL+ will be based on array optics with a VCSEL driver that has a different driving mechanism and is not suitable for single channel transceivers. We advocate and design the dual-channel VCSEL driver with each channel operates up to 10 Gbps. Although both LOClD130 and LOClD65 are dual-channel drivers, each channel in the ASIC is individually powered, making them suitable for applications in dual-channel optical transmitters such as MTx and VTTx or in transceivers such as MTRx and VTRx. LOClD65 is to provide a perfect match to lpGBT when the application does not call for array optics, and to benefit from the current development of optical modules of MTx and VTTx

The analog core of LOClD130 has two parts: a limiting amplifier (LA) and a high-current differential driver. The minimum input signal is assumed to be 200 mVP-P. The LA gain is designed to 14 dB. A shared inductive peaking is used in the 2-stage amplifier to boost the bandwidth to 3.5 GHz. The passive peaking also compensates the high-frequency signal loss due to the ESD pad. Both modulation and biasing currents are programmable with I2C. The total power consumption of one VCSEL driving channel is 56 mW when the modulation current is 6 mA with a 2 mA bias. Power for I2C is below 1 mW.

LOClD65 is similar to LOClD130. Because the input signal is expected to be 100 mVP-P per the lpGBT design specification the LA has 4 stages with shared inductive peaking. An active feedback cell is used between the stages to adjust the gain and bandwidth by programming its current. The feedback cell significantly reduces the process effect on the LA gain and bandwidth. The LA is simulated to have a gain of 18-dB and a bandwidth more than 7 GHz. The output driver has a pre-emphasis option to improve the output signal with different load. The total power consumption of each VCSEL driver channel is 58 mW with 6 mA modulation and 2 mA bias.

Both designs have been verified in simulation and will be submitted for prototype fabrication this summer. We expect to test the chips by the end of this year.

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