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# Time-to-Digital Converter with Adjustable Resolution Using a Digital Vernier Ring Oscillator

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This paper reports the development of a high resolution, low power, and adjustable in frequency Time-to-Digital Converter (TDC), based on two vernier Ring Oscillators (RO) made of standard XOR cells. The TDC is aimed at exploiting the excellent timing performance of the multigap Resistive Plate Chambers (RPC). The frequency of each RO is adjustable thanks to a 9-bit register from 340MHz to 370MHz, allowing theoretically an LSB selection down to one picosecond. The core area measures 35 $\times$75 $\mu m^2$ in a 130nm CMOS technology. Under 1.2V, the TDC consumes 2.3 m$A_{RMS}$ and 260 n$A_{RMS}$ with or whithout signal respectively.

## Summary

A high precision time measurement detected in the RPCs of the high eta muon stations of the Compact Muon Solenoid (CMS) experiment at CERN's LHC is expected to improve the detector performance in the High Luminosity LHC phase.
A Time-to Digital-Converter (TDC) is one of the most crucial building blocks required inside the readout electronics. The exploitation of the TDC performance can be used to reduce the data flow and increase the spacial resolution. High-resolution, better than 10ps, over a nanosecond dynamic range is required. Moreover, the power consumtion has to be limited as well as the jitter (less than 5ps).\\

Other TDC implementation which use inverter delay line or Ring Oscillator (RO) expect a constant delay of each inverter stage. On the contrarty, our novel technique take advantage of every delay cell variation. The period of the Fast RO ($T_F$) and the Slow RO ($T_S$) have $2^9$ combinations each, and their values are randomly spread in a gaussian fit around 2.8ns. The resulting LSB often called
$varDeltaT$ is equal to
$varDeltaT = T_S - T_F$, and could be adjust down to 1ps thanks to this fine tuning. The heart of the RO is made of XOR standard cells, one can thus choose only inverters or buffers as delay elements or a mix of buffers and inverters. A XOR gate delay in the buffer mode is in average 50 ps longer than the inverter mode, the mix of this two families of delay elements can improve the delay time in order to find the best combinaison with the smallest needed delay. This adjustable architecture offers $\frac{512\times513}{2}$ possible ways to configure the two ring oscillators with a random Gaussian fit around zero delay. In principle, the resolution can vary down to 10fs. However, choosing a small LSB ($\Delta t$) implies that the deadtime $\frac{T^2}{\Delta t}$ increases. For robustness issue, a custom Conditional Precharge Flip-Flop (CPFF) has been designed as an optional feature. A minimum setup time of 15ps for the CPFF is measured. Consequently, the phase detector block is characterized using such a CPFF resulting in a $3ps_{RMS}$ S-curve.\\

A prototype of the TDC has been fabricated in 130 $nm$ CMOS technology. The circuit occupies an area of only 35 $\times$ 75 $\mu m^2$ and consumes 2.29 $mA_{RMS}$ with signal and $260nA_{RMS}$ of leakage current without signal. The serial shift register of the ASIC is simply configurable with the spi-pins of a Raspberry-pi plateform to provide all the configuration code to the TDC. The simulated TDC performance could ideally achieves better than 1ps resolution, but the effective measured time resolution performance are limited to 60ps in one nanoseconde depth. The circuit limitation are due to noise jitter accumulation, noise coupling from the power supply and the frequency noise of the ring osillator's itself. However, the proof of concept of this architechture is a success. The limitation of the architecture had been pinpointed and new design of similar improved architecture are under test.

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