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A Digital Processing Unit of a Highly Integrated Receiver Chip for PMTs in JUNO

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The Jiangmen Underground Neutrino Observatory (JUNO) is a multi-purpose underground experiment based on a 20,000 ton liquid scintillator with the one main objective to determine the neutrino mass hierarchy. The signal detection is performed by photomultipliers with directly attached readout electronics. The central component for the digitization process is a receiver chip with a low power analog to digital conversion unit and a large dynamic range. The design and prototype measurements of the included data processing unit and regulation circuits are presented. Additionally, the current status of a model of the receiver chain including future regulation possibilities are shown.

Summary

The Jiangmen Underground Neutrino Observatory (JUNO) is an upcoming neutrino detection experiment located in China that aims to determine the neutrino mass hierarchy by detecting reactor antineutrinos from two nearby nuclear power plants. The central detector is a liquid scintillator with a mass of 20,000 ton and is situated with 700 meters rock overburden. It is surrounded by 18,000 20-inch photomultipliers (PMTs) that are designed to detect the produced light with high timing and energy resolutions while being submerged in water. In order to preserve signal quality and reduce the number of cables in the detector, the receiver chain is integrated into the PMT housing.

A highly integrated analog to digital conversion unit (ADU) is developed in 65 nm TSMC CMOS technology with three high performance 8-bit ADCs that have a programmable gain and run in parallel to achieve a large linear voltage input range of more than 80 dB. After digitization and signal processing, the signal is forwarded above water through a 100 meter Ethernet cable.

Besides the control of the configuration, data processing is a major task in the receiver chip to reduce subsequent processing efforts. This central data processing unit is included in the receiver chip to judiciously select data from one of the three ADCs and to generate metadata to identity the gain of the ADC during data reconstruction amongst other system events like counter overflows. Parallel processing of four samples reduces the effective clock rate from 1 GHz to 250 MHz resulting in a reduction of the power consumption.

Due to the generated metadata, a certain overhead is created that increases the amount of data above the feasible transmission rate. This is countered by a noise data format used during the absence of a signal, achieving a compression factor of two. The resulting difference is covered by an internal buffer which is designed to cover even the most extreme scenarios of increased data rates that occur during galactic supernova events.

A chip prototype adhering to above said specification was designed and fabricated. The data processor was measured by feeding programmed waveforms through an internal waveform generator in the chip. By this, different possible scenarios were fed to the processor and the functionality was successfully verified. The measurement results of the main data processor show the desired data selection scheme and noise compression and will be presented.

To minimize the error due to baseline drifts caused by inter-symbol interference and biasing fluctuations a digital sigma-delta-based ADC baseline regulator is included in the chip. Due to complexity of the analog blocks there are limitations on the possible simulations to verify the regulator, hence a receiver chain model in a high level description platform (MATLAB) is developed. From this system model, the required parameters

are extracted and the ADC baseline offset correction is demonstrated. The system model, the regulator design and the measurement results with the first prototype will be shown.

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