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A 65 nm Macro-Pixel Readout ASIC (MPA) for the Pixel-Strip (PS) Module of the CMS Outer Tracker Detector Upgrade at HL-LHC

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The MPA is the pixel readout ASIC for the hybrid Pixel-Strip module of the Phase-II CMS Outer Tracker upgrade at the High Luminosity LHC (HL-LHC). It employs a novel technique for identifying high transverse momentum particles and provides this information at a 40 MHz rate to the L1-trigger system. The chip also comprises a binary pipeline buffer for the L1-trigger latency, and a data path to support the readout of full events with a maximum trigger rate of 1 MHz and a latency of 12.8 μs. The design and implementation in a 65 nm CMOS technology of the first prototype ASIC that integrates all functionalities for system level operation are presented in this contribution.

Summary

The objective of the CMS Outer Tracker upgrade for the High Luminosity LHC (HL-LHC) is to adopt the use of double layer sensors to facilitate the quick, on-detector, identification of high-pT tracks (>2Gev) and their transmission to the L1 trigger system at the 40MHz bunch crossing rate. For the first time data coming from the Tracker will be used in the L1 trigger decision of a high luminosity hadron experiment. In parallel, a readout channel will transmit triggered events to the DAQ at a nominal average trigger rate of 750kHz.

The Macro Pixel ASIC extracts hits (binary signals) from the pixelated sensor. It comprises a fast front-end with leakage current compensation and amplitude discriminator circuits with binary readout for a 120 x 16 pixel sensor array with dimensions of 23.16mm x 12.0mm. Considering the 1920 channels per chip at a 40 MHz bunch-crossing rate, they represent roughly a data throughput of 80Gbps per chip. Such an amount of data is processed and combined in real time with the input data (2.56Gbps) coming from strip sensor layer in order to identify particles with high transverse momentum. A novel particle recognition algorithm, provides an almost lossless data transmission to the back-end at a bandwidth of 1.6Gbps. This compression combines zero-suppression techniques with the capability of recognizing particles with high transverse momentum. In parallel, every event is stored for a maximum latency of 12.8us and it can be required with a trigger signal. The chip supports a maximum trigger rate of 1MHz and provides the encoded position and dimension of the pixel and strip clusters.

The ASIC is designed in an 8-metal 65 nm CMOS technology. It exploits a Multi-Supply Voltage (MSV) to strongly reduce the digital power consumption without degrading the Analog Front-End and Data transmission performance. Therefore, the digital core is powered at 1V while the Analog Front-End and the custom-sLVS drivers and receivers are powered at 1.2V. The sLVS differential interface utilizes a programmable current to optimize the power consumption while maintaining good signal integrity. The digital core is implemented using standard cell libraries of different threshold voltage devices (Multi-Vt design) to locally improve performance or reduce power consumption. For the distribution of the 40 MHz sampling clock, the chip features a clock distribution scheme based on a clock trunk for the distribution to the pixel rows which allows to achieve a very low clock skew («1ns), while it exploits a clock re-buffering at each pixel row for the system clock to increase the skew and reduce IR drops at the clock transition. The chip clock manager is capable of de-skewing the 40MHz sampling clock to compensate for the particle time-of-flight.
Full chip simulation and power verification show the achievement of the expected performance with a total power density lower than 100mW/cm2.

We will present the design architecture and the development work of the first prototype MPA ASIC integrating all required functionalities for system level operation. The design will be submitted for prototyping in a common full mask set 65nm engineering run with the SSA ASIC.

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