The characterization of a low-power, low-latency, dual-channel serializer ASIC for detector front-end readout

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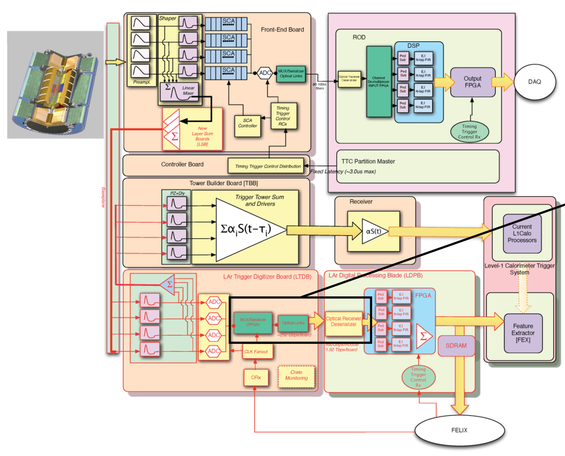
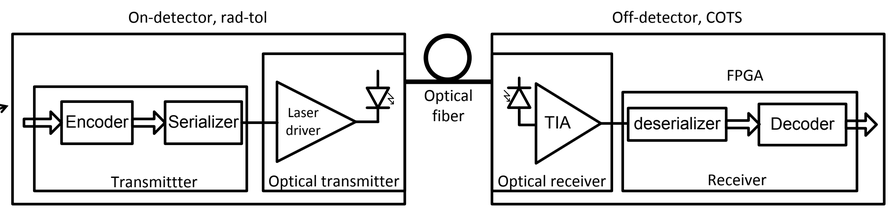
Introduction

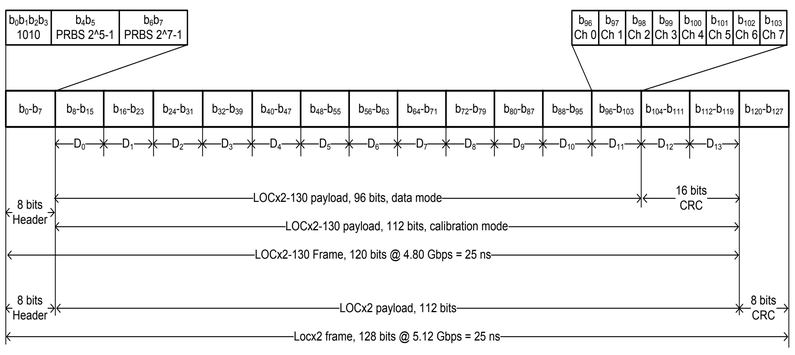




The block diagram of the optical link in ATLAS LAr trigger phase-I update

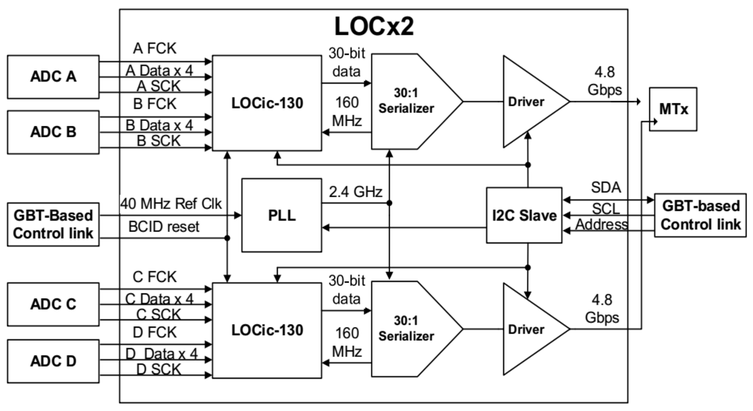
- The ATLAS Liquid Argon calorimeter (LAr) Phase-I trigger upgrade calls for a data transmission rate of 204.8 Gbps for each front-end board (LTDB) [1].
- ASIC serializers are needed for the front-end optical readout due to the demand on data bandwidth, high channel density, low power consumption, low transmission latency and radiation tolerance.
- Based on a commercial 130-nm CMOS process, we have designed a serializer ASIC LOCx2-130 to meet these demands as a pin-to-pin compatible backup of LOCx2.
- LOCx2-130 is a two-channal transmitter ASIC. Each channel receives data from the upstream ADCs [2], encodes the data, and outputs them in serial at a speed of 4.8 Gbps.
- The PLL and the serializer are adapted from a design that originates from the CERN's GBTX ASIC, named as TDS.
- The latency budget of the optical link is 150 ns.
- The power consumption budget of the transmitter ASIC is 1 W.

The design of AISC



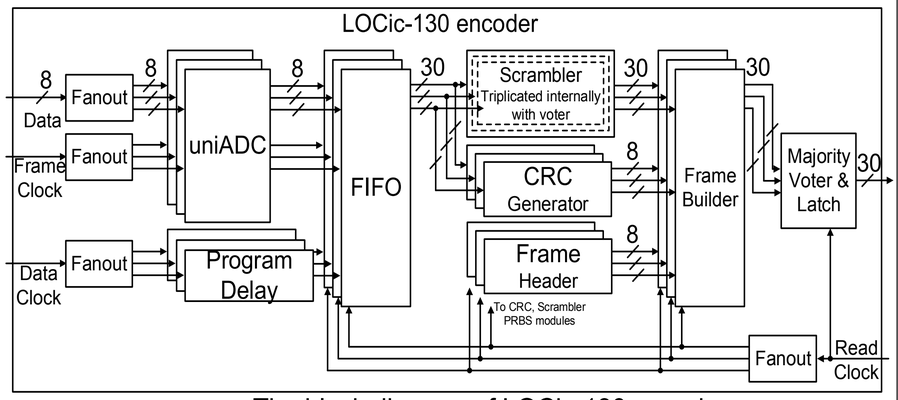
The frame definition of the ASIC LOCx2-130

- The ASIC uses a custom line code called LOCic.
- Each LOCx2-130 data frame has 120 bits, including 8-bit frame header, 96-bit payload and 16-bit frame trailer in data mode or 112-bit payload in calibration mode.
- The payload is scrambled before transmitted, whereas the frame header and the frame trailer are not scrambled.
- 12-bit BCID information is embedded in the frame header.



The block diagram of LOCx2-130 ASIC

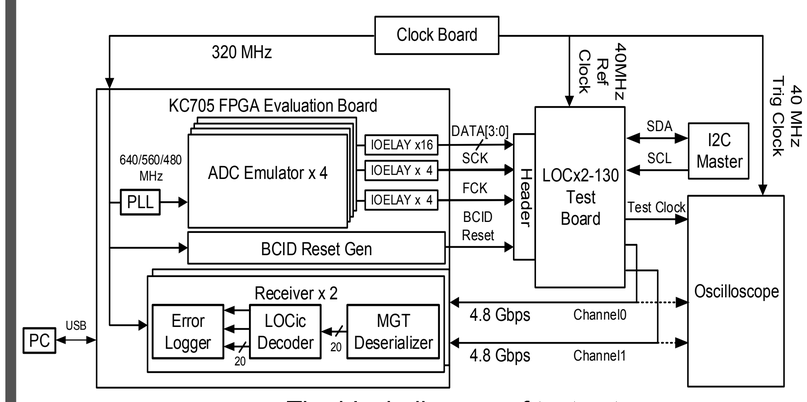
- Each serializer channel of LOCx2-130 takes the digitized data of eight analog signals from two ASIC ADCs or one ADS5272 or one ADS5294.
- LOCx2-130 is composed of two encoders, two 30:1 serializers, two drivers, a shared PLL, and an I2C slave.
- The latency of the LOCx2-130 is power on independence.



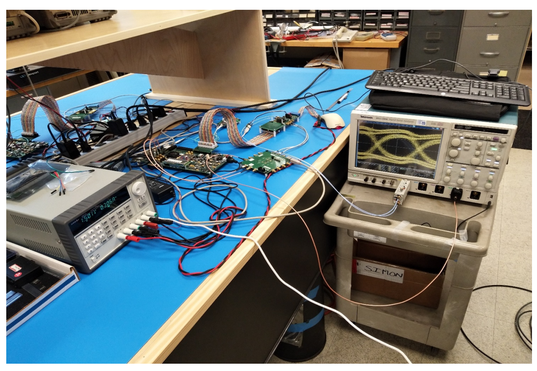
The block diagram of LOCic-130 encoder

- The encoder is composed of an ADC interface, a synchronous FIFO, a PRBS generator, a CRC generator, a scrambler, and a frame builder.
- The Verilog code of LOCic-130 is triplicated. Modules that have pipeline structure without internal feedback like FIFO and Frame Builder or modules that do have the internal feedback but are reset periodically like the CRC and the Frame Header are simply instantiated by three times as triple redundancy.
- The Scrambler however, has feedback and no reset mechanism, is triplicated internally with the voter added at the input of every D flip-flop to eliminate errors, therefore, the error will not be latched in the D flip-flop and cause permanent malfunction.

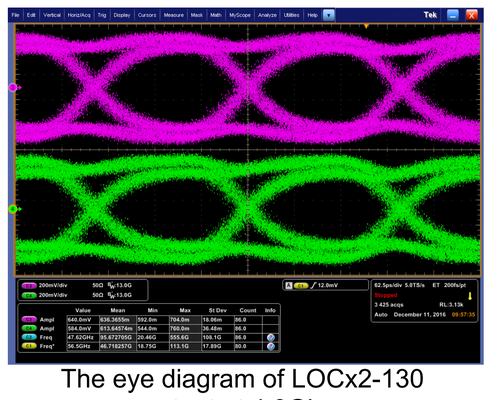
The test system and measurement results



The block diagram of test setup



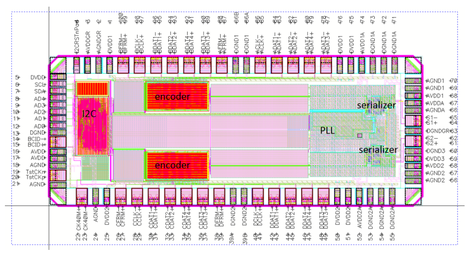
A picture of test setup



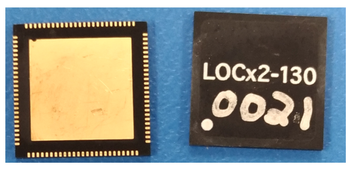
The eye diagram of LOCx2-130 output at 4.8Gbps

Serial data output rise time	78.4 ps
Serial data output fall time	78.4 ps
Serial data output deterministic jitter	28.1 ps
Serial data output random jitter	2.3 ps (RMS)
Serial data output total jitter	52.1 ps (peak-peak)
Serial data output amplitude	300 mV (peak-peak)
Serial data output BER	$< 10^{-12}$
Total power consumption of LOCx2-130 chip	440mW

LOCx2-130 measurment



Layout of the LOCx2-130 ASIC



QFN packaged LOCx2-130 ASIC

Simulation Measurement

Function block		Latency (ns)
TX	FIFO	16.4~22.7
	Scrambler & CRC gen	0.0
	Frame Builder	6.3
	Serializer	11.7
	Total LOCx2-130	34.4~40.7
RX	Deserializer	36.7~40.1
	Data Extractor	12.5
	Descrambler	4.2
	CRC Check	4.2
	Total FPGA	57.5~60.9
Total optical link		91.9~101.6

Latency of the optical link

Conclusion and outlook

- An serializer ASIC, LOCx2-130, is designed and tested for the ATLAS LAr Calorimeter trigger upgrade.
- LOCx2-130 consists of two channels and each channel encodes ADC data and transmits serial data at 4.8 Gbps with a latency of less than ns. The power consumption is 440 mW.
- The dies of LOCx2-130 will be fabricated in an engineering run this autumn.

Acknowledgments

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References

[1] ATLAS Collaboration, *ATLAS liquid argon calorimeter Phase-I upgrade technical design report*, CERN-LHCC-2013-017 and ATLAS-TDR-022, September 20, 2013.
[2] J. Kuppambatti, et al, A radiation-hard dual channel 4-bit pipeline for a 12-bit 40 MS/s ADC prototype with extended dynamic range for the ATLAS Liquid Argon Calorimeter readout electronics upgrade at the CERN LHC, 2013 JINST 8 P09008

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