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The Characterization of a Low-Power, Low-Latency, Dual-Channel Serializer ASIC for Detector Front-End Readout

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We present the design and test results of LOCx2-130, a low-power, low-latency, dual-channel serializer ASIC for detector front-end readout. LOCx2-130 consists of two serializer channels with custom encoders and each channel operates at 4.8 Gbps. The ASIC is fabricated with a commercial 130-nm CMOS process and is packaged in a 100-pin QFN package. LOCx2-130 consumes 440 mW and achieves a bit error rate of below 10-12 with a latency of from 34.4 ns to 40.7 ns.

Summary

ASIC serializers are needed for the front-end optical readout due to the demand on data bandwidth, high channel density, low power consumption, low transmission latency and radiation tolerance. Based on a commercial 130-nm CMOS process, we have designed a dual-channel serializer ASIC LOCx2-130 to meet these demands, in particular in the ATLAS Liquid Argon Calorimeter Phase-I trigger upgrade.

LOCx2-130 has two serializer channels and each channel operates at 4.8 Gbps. The two channels share a PLL. Each channel has a custom data encoder called LOCic and a serializer. The LOCic receives the data from the upstream ADCs to form data frames and is digitally synthesized with the transmission latency optimization. The LOCic is protected with the triple modular redundancy (TMR) technique. LOCx2-130 can interface one out of three types of ADCs, a 12-bit ASIC ADC, a 12-bit commercial ADC ADS5272 and a 14-bit commercial ADC ADS5294. A synchronous Fist-in-First-Out (FIFO) accommodates a clock skew of up to 3.125 ns between the two ASIC ADCs. The serializer and the PLL are adapted from a design that originates from the CERN' s GBTX ASIC. We slightly modified the design to share a PLL between two serializers. The GBTX designer Paulo Moreira reviewed the whole design of LOCx2-130.

LOCx2-130 has been packaged in a 100-pin plastic quad-flat no-leads (QFN) package and has been evaluated. The test system consists of a test board and a Kintex-7 FPGA. The FPGA implements ADC emulators (ASIC ADC, ADS5272 and ADS5294) as the input of the LOCx2-130 test board. The FPGA-embedded input/output delay modules are used in the ADC emulators to ensure signal alignment. The FPGA also implements two link receivers. Each link receiver includes the deserializer of a Multiple-Gigabit Transceiver (MGT), a LOCic decoder, and an error logger. The deserializer converts the 4.8 Gbps serial data stream into parallel data. Then the LOCic decoder recovers the original ADC data and checks if there are errors in the recovered data. The error logger records error types and time stamps.

Our test shows the power consumption of LOCx2-130 is 440 mW at the design speed of 4.8 Gbps. In the link test, the receiver implemented in the FPGA identifies the date frame boundary correctly and the frame data passes the CRC check. The output of the serializer passes the eye mask test with a bit error rate of below 10-12. The latency of the whole link, including the receiver and the serializer, is from 100.2 to 106.2 ns and the chip latency is from 34.4 ns to 40.7 ns. As expected, the serializer tolerates 3.125 ns clock skew between two input ASIC ADCs. Irradiation tests will be carried out in the coming months and will be presented in the workshop and in the proceeding.

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