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ASICs and Readout System for a High Resolution UV Single Photon Imagining Detector

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Large aperture MCP based UV single photon imaging detectors are commonly used in space applications. NASA granted,the development of new detector with a geometrical acceptance up to a 100x100 mm, as well as ASICs for the construction its readout system. We developed the detector and ASIC chips which enabled the construction of it's readout system. The system is composed of fast, low noise and low power 16ch CSA amplifier ASICs, and 16ch waveform sampling GSPS ASICs. The detector and readout system are currently under evaluation, meanwhile a novel and even more compact readout system on chip is undergoing design process.

Summary

The Department of Physics and Astronomy (ID Lab) at University of Hawai'i and Space Sciences Laboratory, Berkeley, collaborate on the development of a UV single photon imaging detector with crossed strip readout. The detector uses a photo-cathode to convert single photons into photo-electrons and an MCP stage for charge multiplication. The photon income position is extrapolated by measuring the charge cloud distribution over orthogonal anode strips being 25um wide and 625um apart. Our base line detector has an aperture of 50x50mm, hence the readout system needs to measure 160 channels. Using an older laboratory readout system, a spatial resolution of 17um FWHM was measured [1]. Space grade instruments require to operate at very low power, low noise and enable high count rate.

We developed a 16 channel charge sensitive amplifier (CSA) ASIC [2] in 130 nm TSMC-CMOS technology. It features a linear range up to 50fC, baseline gain of 10mV/fC, noise figure of ~600e-, analog pulse rise time of 25ns, and power consumption of ~5mW per channel. Its partnering ASIC, called Half-Graph, is a 16 channel waveform sampling and digitizing GS/s ASIC. The sampling capacitor array, along with an analog storage array, enables to keep about 8 us of data per channel. An external FPGA is used to access the analog memory array and convert the stored values using the ASIC internal 12 bit slope converter. Converting only the data of interest enables efficient data throughput, hence a high single photon count rate. It is designed in 250nm CMOS technology. Both chips have being recently irradiated with gamma rays. The CSA sustained 850kRad dose without notable degradation. The HalfGraph was irradiated with 225kRad without observable issues. Both could qualify for Jupiter missions with appropriate shielding, where the requirement is to functionally pass a dose of 200kRad.

Both chips are programmable to reduce required external biasing components for operation. Using these ASICs we constructed a scalable self trigged readout system, which is presently under evaluation coupled to the 50x50 mm detector. The 160 channel system constitutes of 10 CSAs and 10 Half-Graphs. The power consumption ranges around 12W, and this number includes as well 2 ARTIX 7 FPGAs required for controlling the system. A new 100x100mm aperture detector along with a scaled readout system are under construction.

To further decrease the power consumption, reduce the system complexity and shrink the package footprint, we design a new ASIC called GRAPH. This ASIC will encapsulate a CSA and a GS/s ADC on a single die using 130nm TSMC technology. We present the ASICs and the readout system for the 50x50 mm detector, obtained results and share details on the GRAPH architecture.

[1] J. Vallerga et al., " Development of a flight qualified 100 x 100 mm MCP UV detector using advanced cross strip anodes and associated ASIC electronics ", Proc. SPIE 9905, Space Telescopes and Instrumentation 2016

[2] A. Seljak et al., A fast, low power and low noise charge sensitive amplifier ASIC for a UV imaging single photon detector, JINST 2017

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