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FED Firmware Interface Testing with Pixel Phase 1 Emulator

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A hardware emulation of the CMS pixel detector phase 1 upgrade front-end electronics was developed to test and validate the architecture of front-end driver (FED) firmware. The emulation, implemented on the CERN GLIB uTCA platform, drives optical transmitters to the back-end electronics. The firmware emulates the complex functions of the readout chips and Token Bit Managers and allows for possible exceptions in the output data. The emulation implements fixed data patterns and realistic simulated data to drive readouts at expected data and trigger rates. Testing software was developed to control and verify correct transmission of data and exception handling in the FED.

Summary

The pixel phase 1 upgrade has been installed in the CMS detector. The pixel detector modules are made up of two layers, a thin silicon layer and a readout chip that is bump bonded to the silicon pixels. The silicon pixel system is a reverse p-n junction that allows charged particles to create electron-hole pairs to measure the charge. This new detector includes an added detector layer for both the barrel and forward pixels. Along with a high efficiency readout chip (PSI46digv2 and PROC600) and increased precision for tracking and vertexing. The increased luminosity of the LHC in Run 2 will lead to a large expected data rate and therefore a high bandwidth front-end driver (FED) to manage the data. A CERN gigabit link interface board (GLIB) with Virtex 6 FPGA customized firmware and software is used to probe the features of new FED firmware releases. By exploiting an 8-way SFP FPGA Mezzanine Card a single GLIB can emulate 16 independent channels of the phase 1 pixel detector. Output from the pixel detector is converted from two 160 Mbps signals to one 400 Mbps optical output using bitwise interleaving and non-return-to-zero inverted (NRZI) encoding. The GLIB is used to emulate all layers of the pixel detector in multiple configurations to stress the FED. Many possible exceptions can be generated and read out such as, bit flips, missing event headers/trailers, and delayed events. Possible scenarios are out-of-sync due to event number error or timeout and missing events due to missing the event header. Utilizing these functions, it is possible to generate unlikely events or recreate conditions that are seen in the detector to probe the processes in the FED readout. Data can be sent in fixed event sizes or from simulated events that are locally stored on the GLIB. Using a FEROL 10 G link, realistic simulations of pileup of 70 and 130 can be read out at 2.4 Gbps at 100 kHz and 3.9 Gbps at 86 kHz, respectively. Larger data rates are possible, but the trigger rate is throttled by the AMC13. An installation has been integrated into the pixel DAQ test system at CMS for fast verification of FED firmware upgrades.

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