# Studies on the readout of the ATLAS Inner Tracker using commercial networking hardware

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## Introduction

In the course of the HL-LHC upgrade (2024-2026) with expected luminosities of up to $5 \cdot 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ ATLAS will perform the Phase-II upgrade. During this upgrade the complete Inner Detector of ATLAS will be replaced by the new **I**nner **T**rac**k**er (ITk).
One possible layout for the ITk is shown in Figure 1. It consists of a pixel detector with five barrel layers and four end-cap rings and a silicon strip detector with four layers and six end-cap disks. This layout provides 9 space points up to $|\eta| \approx 4$.The planned pixel size is $50 \times 50\,\mu\mathrm{m}^2$ in the pixel detector. During the full operation time of the ITk detector the innermost layer has to withstand a total ionizing dose of about $50\,\mathrm{MGy}$.
Also the ATLAS trigger system will be upgraded for Phase-II. Currently, there are two possible options how the trigger system for Phase-II will look like. The first option would be a two stage trigger system (L0 at $1\,\mathrm{MHz}/10\,\mu\mathrm{s}$ latency, L1 at $400\,\mathrm{kHz}/60\,\mu\mathrm{s}$ latency) with a hardware track trigger system as input for an L1 trigger decision. Another option is the full readout at an increased L0 rate (up to $4\,\mathrm{MHz}$ are under discussion) and a maximum latency of $25\,\mu\mathrm{s}$. In this version the track triggering would be handled in software.
With a planed readout speed of $5.12\,\mathrm{Gb/s}$ per link, up to 2 links per module and around 10 000 modules, a combined data rate in the order of $100\,\mathrm{Tb/s}$ is expected. This amount of data needs to be taken care of within the fixed constrains (like space, power and money) given. Therefore, our proposed solution is based on rather simple nodes, being able to be packed into high density crates and using commercial networking parts. These nodes are also planed to be operated in standalone mode for production tests as well as laboratory or test-beam usage.
Finally, the system follows the ATLAS TDAQ approach using interface cards between the detector and the network (FELIX). Therefore, the system can provide a beneficial input for developing the final ITk readout system. As the strategy of detector connection is the same, critical topics can be studied and development of firmware and software which is needed for the detector specific operation tasks, as they are calibration and data taking, can be started.

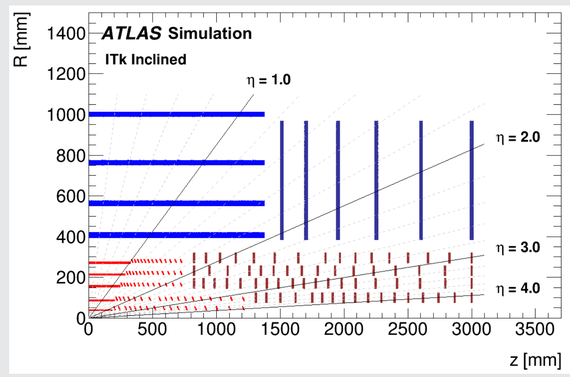


**Figure 1:** Possible ITk layout as presented in [1], with 9 space points up to $|\eta| \approx 4$ consisting of a pixel detector (red) and a silicon strip detector (blue).

## Data Flow Scheme

A local trigger interface provide access to the central trigger information like trigger IDs and forwards feedback signals like busy back to the central infrastructure. The calibration and run configuration are received via commercial networks. All these information are combined in the readout card, encoded in the frontend specific protocol and send out to the detector.

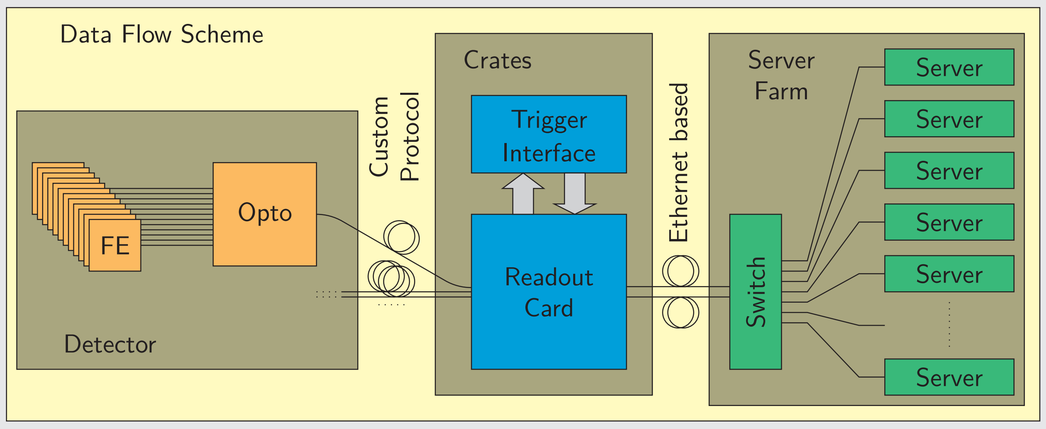


**Figure 2:** Data transmission scheme forseen to be used in the ITk Pixel Detector.

The data coming back from the detector is received by the readout card through optical fibers. The custom protocol is decoded partially for a first error check. After this, the combined data from the different links is packed into packets and sent out using commercial networking protocols.
To maximize the performance and to reduce the number of needed parts at the same time, the $10\,\mathrm{Gb/s}$ network interface is realized within the FPGA. Support for $40\,\mathrm{Gb/s}$ operation is in development and a $100\,\mathrm{Gb/s}$ version is planned.

The network stack includes the follow features:

- Ethernet, ARP, IPv4, ICMP (echo request/reply), UDP
- easy integration of additional protocols due to open interfaces (AXI Streaming [6])
- support for jumbo frames (limited only by IPv4 length field)

Not implemented are:

- support for fragmented IPv4 packets, IPv4 options and QoS
- reliable transport protocols like RUDP or TCP

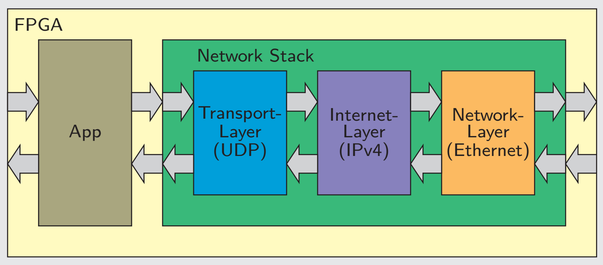


**Figure 3:** The building blocks of the network stack which is included in the readout card.

## Measurements

In the plot below, the achieved payload bandwidth for different packet sizes is depicted. We sent a UDP/IP stream from a FPGA board to another FPGA board (the purple line) and from the FPGA to a PC (green line). We also tried a Xilinx example design [5] using the ARM processor within the FPGA SoC as comparison (blue line).

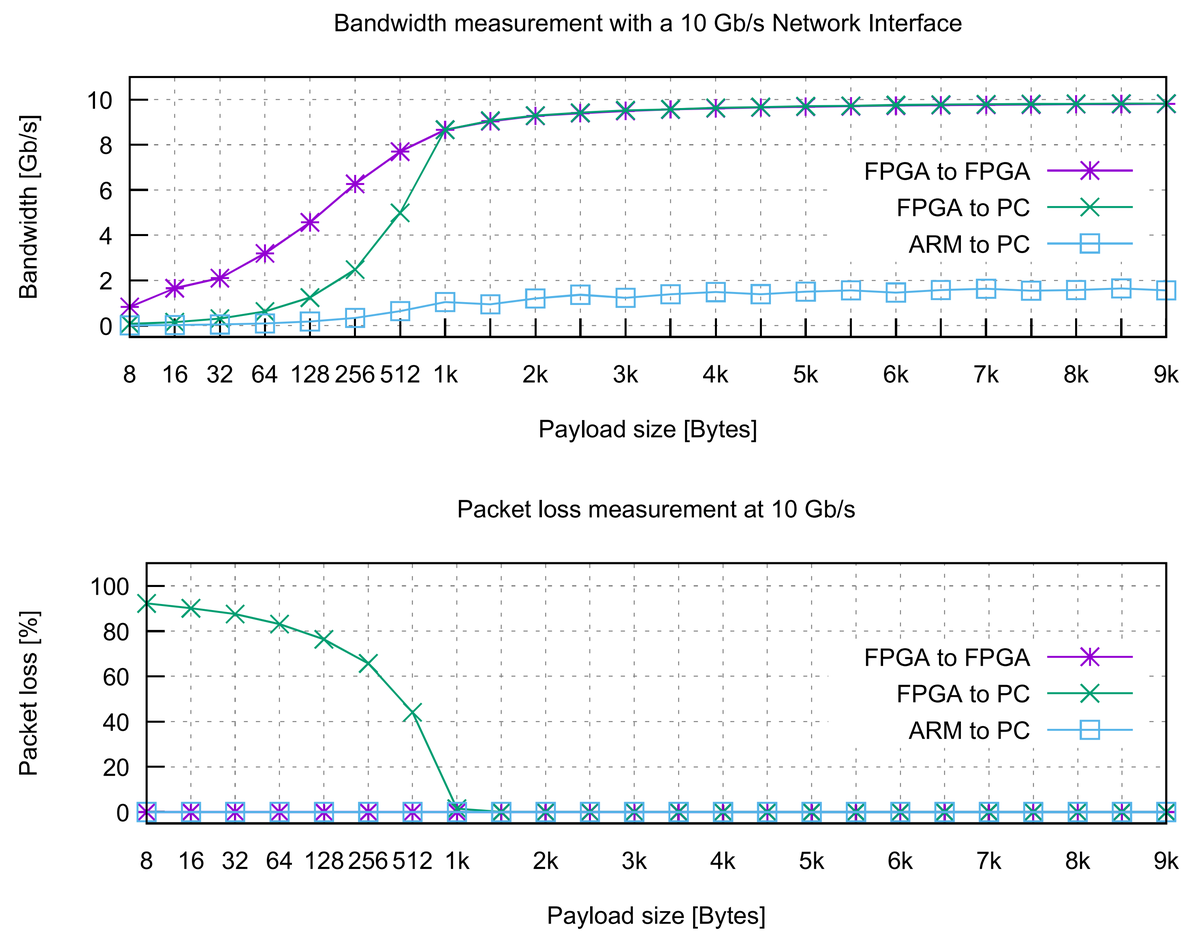


**Figure 4:** Results from performance measurements for FPGA to FPGA, FPGA to PC and ARM to PC tests.

## Application

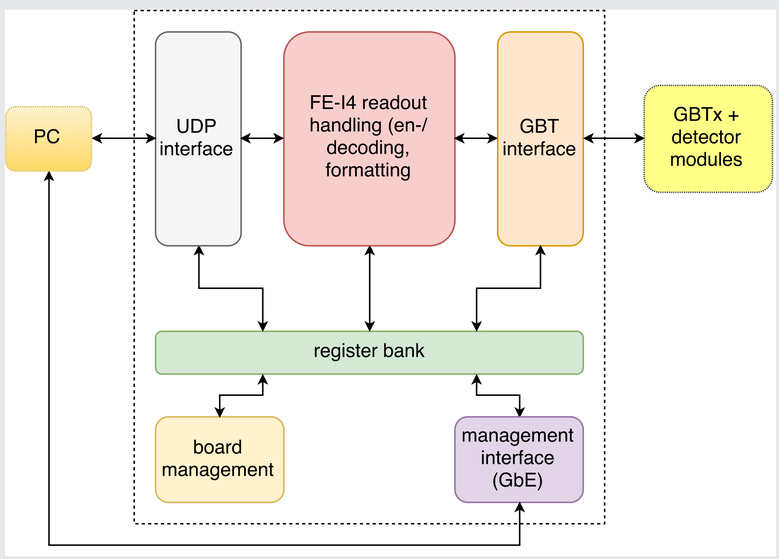


**Figure 5:** Block diagram of the readout card firmware.

- ITk demonstrator system test will be installed at CERN and will use FE-I4-based [2] detector modules (total number of front-ends: 120).
- GBT ecosystem [3] will be used as optical data link with 4.8 Gb/s data rate including a forward-error-correction.
- System test can be used to evaluate readout system with high-speed optical data links.
- "Off-Detector" readout system based on Avnet Kintex-Ultrascale Evaluation board [4] has been developed.
- Block diagram of the firmware is shown in Figure 5. Central part is the front-end handling firmware plus supporting blocks for the GBT and UDP communication.
- Currently support for one GBT link and one 10 Gb/s Ethernet link.
- Data from the front-end chips will be shipped out via UDP on the 10 GbE interface to a server PC through a switched network.
- Integration of the readout system into the future ITk readout software framework is under preparation and a first implementation is available.
- Calibration procedures can be executed through the high-level software. A digital injection scan with a single front-end chip is shown in Figure 6. Gaps in the scan refer to lost packets.
- Outlook:
  - Large scale system supporting 8 GBT links (equal to 160 FE-I4s) and two 10 GbE interfaces under preparation.
  - Improvement of the UDP reliabilty required (e.g. resend mechanism).

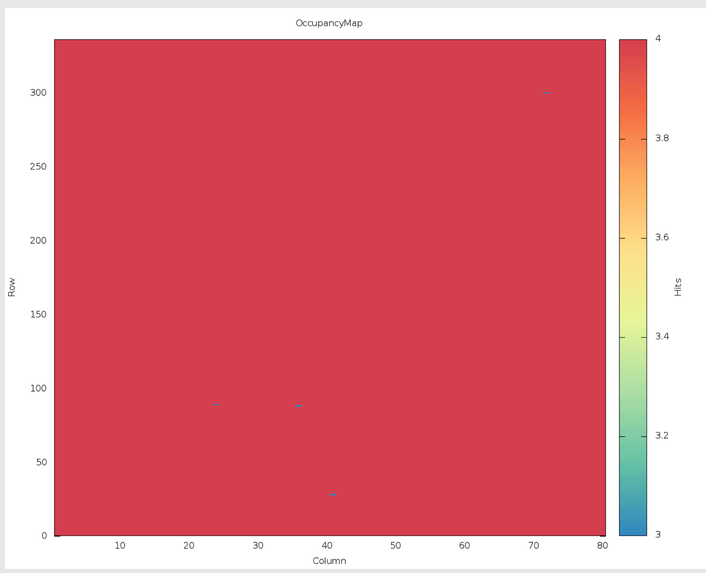


**Figure 6:** Result of a digital injection scan with a single front-end chip. Gaps in the scan refer to lost packets.

## References

[1] The ATLAS Collaboration, Technical Design Report for the ATLAS Inner Tracker Strip Detector, CERN-LHCC-2017-005 CERN (2017), https://cds.cern.ch/record/2257755.

[2] M. Karagounis et al., Development of the ATLAS FE-I4 pixel readout IC for b-layer upgrade and Super-LHC, CERN-2008-008:70-75, https://cds.cern.ch/record/1158505.

[3] Moreira, P and Marchioro, A and Kloukinas, The GBT: A proposed architecure for multi-Gb/s data transmission in high energy physics, CERN-2007-007:332-336, https://cds.cern.ch/record/1091474.

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[5] Xilinx, PS and PL-Based 1G/10G Ethernet Solution, XAPP1305 (v1.0) March 24, 2017, https://www.xilinx.com/support/documentation/application_notes/xapp1305-ps-pl-based-ethernet-solution.pdf.

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