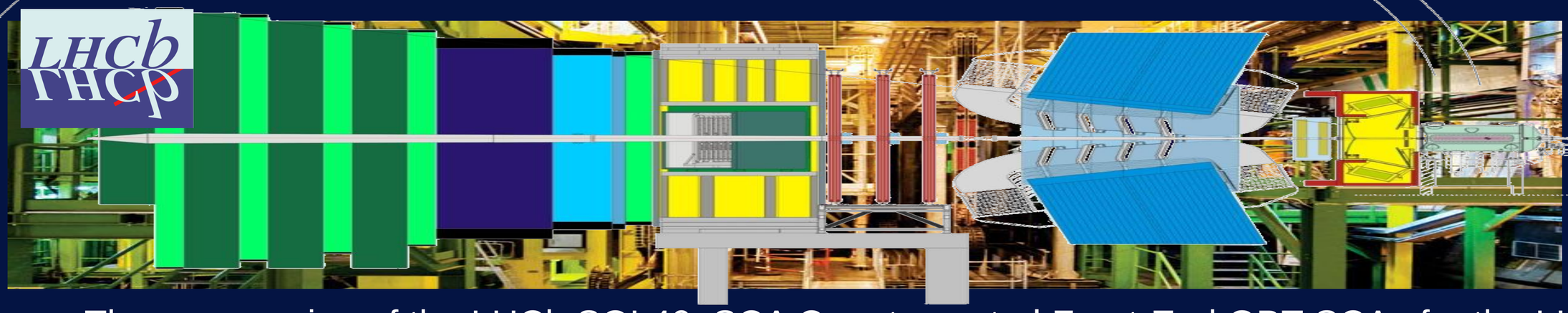


CERN Organisation
Europeenne pour la Recherche
Nucleaire
CH-1211 Geneve 23
Switzerland

The new version of the LHCb SOL40_SCA Core to control Front-End GBT-SCAs for the LHCb Upgrade

João Barbosa, Federico Alessio, Clara Gaspar
CERN, Geneva, Switzerland

Introduction

LHCb collaboration is now preparing for the 2020 upgrade [1]:
- no hardware trigger for data acquisition (40 MHz readout)
- Trigger-less Front-End electronics
- 40 Tb/s data acquisition network

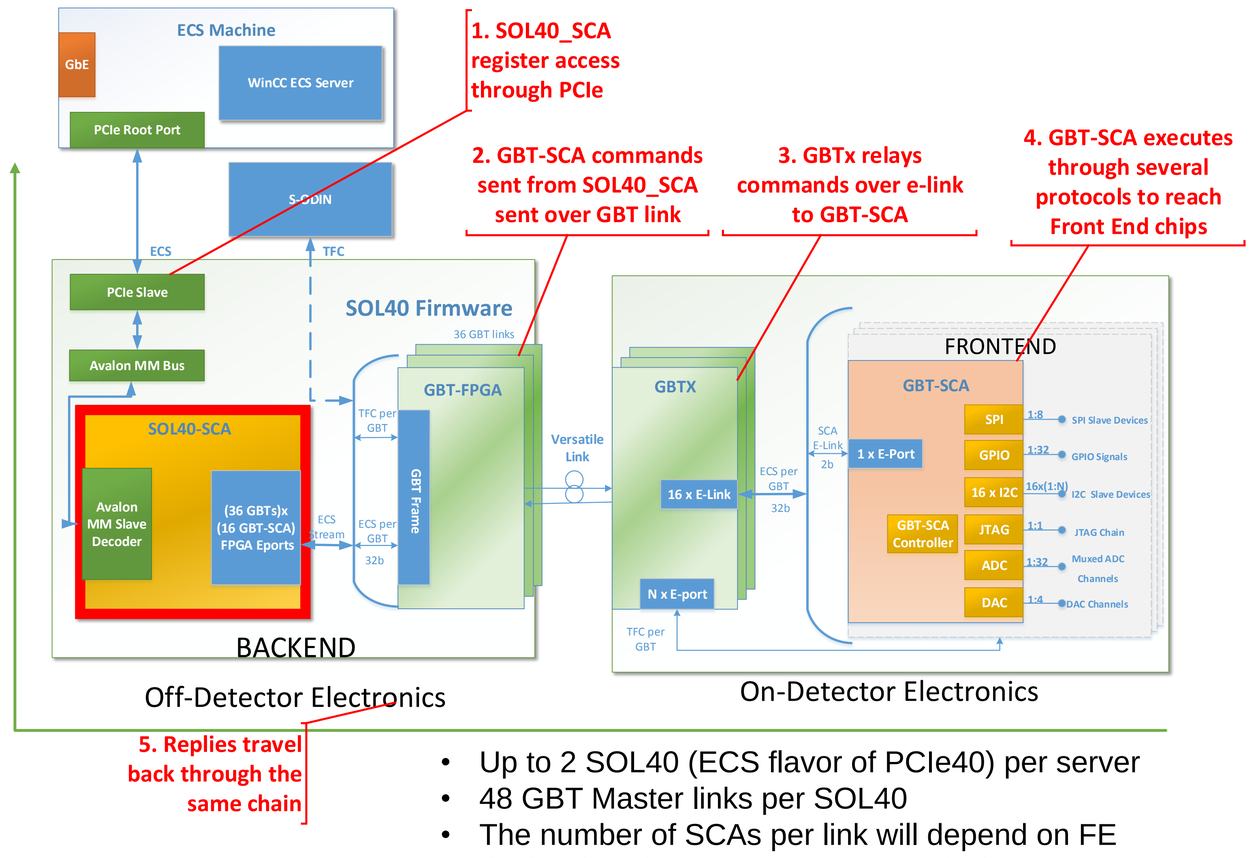
Gigabit Transceiver (GBT) chipset used in new Front-End Electronics for Data Acquisition (DAQ), Timing and Fast Control (TFC) [2], Slow Control (Experiment Control System – ECS) [3].

PCIe gen 3 FPGA based boards (PCIe40) interface GBTx [4] and TFC/ECS for high bandwith bidirectional communication
- LHC clock distribution
- 40MHz commands (synchronous and asynchronous)
- ECS bidirectional data (commands and monitoring)

40 PCIe40 boards interface ~2500 GBTs and GBT-SCAs as well as 10k FE chips.

SOL40_SCA firmware core [6] create to control GBT and GBT-SCA. Tests unveiled a need of a faster, more efficient and lightweight core.

ECS Data Path



- Up to 2 SOL40 (ECS flavor of PCIe40) per server
- 48 GBT Master links per SOL40
- The number of SCAs per link will depend on FE design (maximum 32, most cases 2-6)

Motivations for Upgrade

Resources for 1 link instance and 17 SCAs (48 link estimate) in Arria 10

Entity	ALMs out of 427200	Dedicated Logic registers	Memory block bits
48 link instantiations *	491640 (110%)	426480 (40%)	5374848 (10.6%)
Top	10242.5 (2.3%)	14255 (.8%)	122856 (.22%)
Interface layer	284.7	554	0
Buffer Layer	991.5	2001	105448
Protocol Layer	3484.7	3108	0
Mac Layer	5633.2	9325	18496
Mac Layer per SCA	342.6	537	1088

*Estimate assuming linearity

1) Not enough space in Arria 10 for 48 link instances. Logic is replicated per link, can be avoided.

2) Software tool has to probe for a reply at every command it sends, delaying new commands.

3) Too dependent on the performance of the host server for command packaging.

Proposed solution:

- Make the new SOL40_SCA core support several GBT master links.
- Implement more complex ECS commands for the different GBT-SCA protocols, mainly I2C, JTAG and SPI.
- Make extensive use of memories available in the device:
  - Better command and reply buffering.
  - Memory configuration and periodical triggering of saved commands.
- Improve scaling of resource usage with the number of SCAs supported.

FPGA remote configuration tests

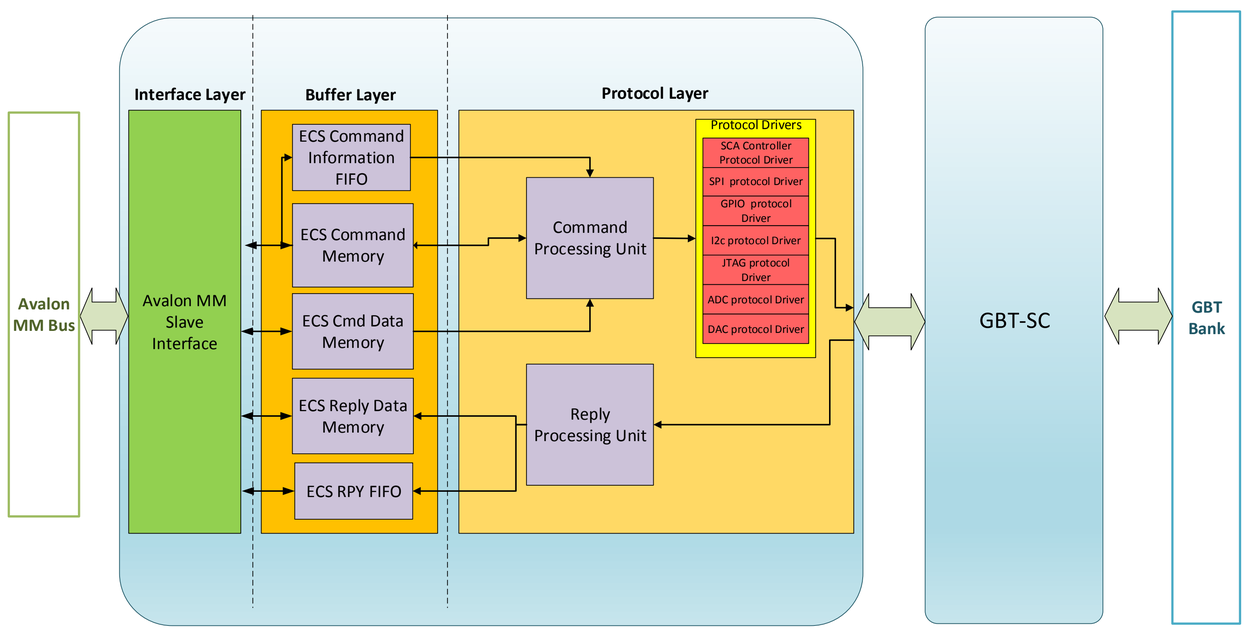
These tests performed with the current version of the SOL40_SCA for the GBT-SCA JTAG.

Host PC CPU	Intel(R) Atom(TM) CPU E640 @ 1.00GHz	Intel(R) Xeon(R) CPU E5-2630 v3 @ 2.40GHz (target system)
On Board FPGA	Stratix V 5SGXEA7N2F45C3N GX	Arria10 10AX115S4F45E3SG
Interface	PCI Express Gen 1	PCI Express Gen 3
JTAG speed (no encoding)	18 KB/s	267 KB/s
JTAG speed (5x encoding)*	87 KB/s	405 KB/s
Speedup	4.8x	1.51x

* 5 GBT-SCA commands sent per ECS command

Current architecture is now successfully used to configure FPGAs through the GBT-SCA (namely Xilinx Series 7 family and Microsemi's IGLOO2 and SmartFusion2).

SOL40_SCA Version 2



New features:

- Data separated from commands so it can be reused
- Decoupled Reply and Command chain to minimize waiting time
- Protocol accelerators are generated on user demand.
- Expected throughput in data channels of GBT-SCA (I2C, JTAG and SPI) of ~500 KB/s
- Each core supports several GBT master links
- Using GBT-SC core provided by the CERN Eletronics Group (EP-ESE).

References

[1] Liu, G., and Neufeld, N (2014). *DAQ architecture for the LHCb upgrade*. *Journal of Physics: Conference Series*. Vol. 513. No. 1. IOP Publishing.
[2] Alessio, F., et al (2016). *Timing and Readout Control in the LHCb Upgraded Readout System*. No. LHCb-PROC-2016-015.
[3] Alessio, F. et al. (2010). *The LHCb Run Control System,* Real Time Conference (RT), 2010 17th IEEE-NPSS, Lisbon, 2010, pp. 1-6.
[4] Moreira, P. (2013), *The radiation hard GBTX link interface chip.* PH-ESE Electronics Seminars, November. Vol. 26.
[5] Bellato, M., et al. (2014), *A PCIe Gen3 based readout for the LHCb upgrade.* Journal of Physics: Conference Series. Vol. 513. No. 1. IOP Publishing.
[6] Alessio, F. (2015), et al. *A generic firmware core to drive the Front-End GBT-SCAs for the LHCb upgrade.* Journal of Instrumentation 10.02: C02013.