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An FPGA-Based Sampling-ADC for the Crystal Barrel Calorimeter

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The digitization stage of the main electromagnetic calorimeter of the CBELSA/TAPS experiment in Bonn (Germany) is being equipped with custom 80 MSPS, 14 bit Sampling-ADCs. Onboard data processing with FPGAs allows determination of the signal characteristics, reducing the data substantially. The readout of the unprocessed sampling data allows offline analysis and refinement of the FPGA-algorithms.

A partial setup has shown promising results during a photoproduction-beamtime. It has been demonstrated that the SADCs are able to overcome the readout-rate limitation of the current QDC readout.

The full setup is planned to be commissioned within the next year.

Summary

The main electromagnetic calorimeter of the CBELSA/TAPS experiment has been equipped with a new Avalanche-Photodiode readout to obtain full trigger capability. Within the scope of this modification, the digitization stage of the energy branch is upgraded from Fastbus QDCs to custom Sampling-ADCs to gain a higher readout-rate.

The design has been adapted from the PANDA-SADC that is being developed by P. Marciniewski. A low noise switching power supply, as well as an analog input stage with multi-feedback filters, digitally controllable pole-zero compensation and baseline-shifting have been developed. Furthermore, a custom backplane was added for distribution of trigger, clock (phase) and slowcontrol.

The SADC features 64 channels with 14 bit and 80 MSPS in a NIM 1/12 cassette, with a power consumption of 22 watts. Two Kintex 7 FPGAs process the digitized signals onboard. Data is transferred with two 1Gbit/s UDP/IP copper links to COTS switches with 10Gbit/s uplinks. Event-buffering and -building is done in conjunction with a linux server system.

For the full readout of the calorimeter, two NIM crates will be equipped with SADCs, yielding 1536 channels; enough for the maximum of 1380 signals from the calorimeter as well as 60 fast energy sum signals. The full dynamic range of each channel is 2.5 GeV.

As the bandwidth of the processed CsI(Tl) scintillator crystal signals barely extends above 1MHz, the sampling rate is decimated by a factor of four, yielding a vertical resolution of 16 bit. The waveform data is reduced by means of further FPGA processing upon external or self trigger. Methods used for determination of timing and energy include digital constant fraction discrimination, integration and peak detection. Algorithms for pile-up determination ensure the recovery of previously discarded energy signatures. For the case of detected pile-up, and as a means of debugging, the readout of full samples is possible. Offline-analysis of the full samples has proven helpful for the refinement of the FPGA algorithms.

A preliminary setup, reduced to one quarter of the full calorimeter, has been operated during two early commissioning meson-photoproduction-beamtimes at the ELSA (Electron Stretcher Accelerator) facility in April and June 2017. The quality of the data has proven to be at least competitive to the existing QDC readout. Kinematic analysis have shown the expected signatures of $\pi0$- and η-mesons. The possibility of the oscilloscope-like access to all signals has been valuable for detector diagnosis during the beamtimes.

The readout-rate is limited mainly by the UDP/IP implementation and the necessary custom software-handshake to ensure data integrity. Yet, above 10 kHz readout rate have been obtained already, with room for further optimizations; whereas the current readout is limited to 1 kHz.

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