# Low voltage powering of on-detector electronics for HL-LHC experiments upgrades

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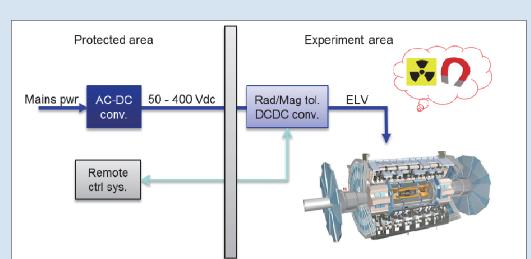
## Introduction

All LHC experiments will be upgraded during the next LHC long shutdowns (LS2 and LS3). The increase in resolution and luminosity and the use of more advanced CMOS technology nodes typically implies higher current consumption of the on-detector electronics. In this context, and in view of limiting the cable voltage drop, point-of-load DC-DC converters will be used on detector. This will have a direct impact on the existing powering scheme, implying new AC-DC and/or DC-DC stages as well as changes in the power cabling infrastructure. This poster presents the first results obtained while evaluating different LV powering schemes and distribution layouts for HL-LHC trackers. The precise low voltage power source requirements are being assessed and understood using the CMS tracker upgrade as a use-case.

# Scope of the project

#### **Current situation of LV powering in the experiments**

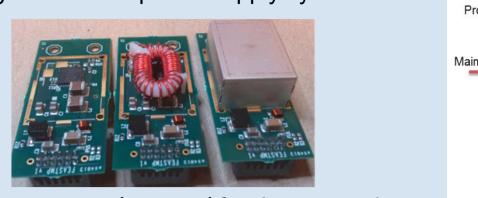
- PS in counting house and/or experimental cavern (distributed system in most cases) Use of linear regulator on certain detectors
- Certain PS equipment in harsh environment (Radiation and B-field)
- Extra low voltage (ELV) as well as
- low noise and ripple requirements Custom PS systems
- Complex (water cooling,
- magnetic shielding, etc.) o Constrained (e.g. limited remote monitoring)
- Costly



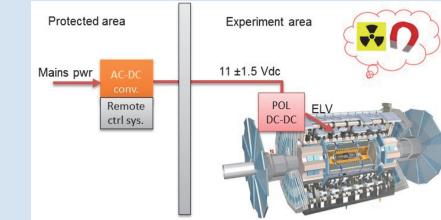
Typical powering configuration in running LHC experiments

# **Project objectives**

- Explore, simulate and compare different powering solutions for systems based on POL DC-DC converters.
- Assess and understand the low voltage power source requirements.
- Evaluate and simulate the dynamic behaviour of the entire powering chain.
- Characterize the explored solutions and draft technical specifications towards the next generation of power supply systems.



POL DC-DC converter (FEASTMP) for phase I upgrades



The supply of POL DC-DC converters at 12V makes it possible to consider relocating power supplies to the service caverns, and thus avoid the costly development and constrained maintenance conditions of radiation and magnetic filed tolerant converters. The feasibility demonstration of this powering scheme was one of the objectives of this

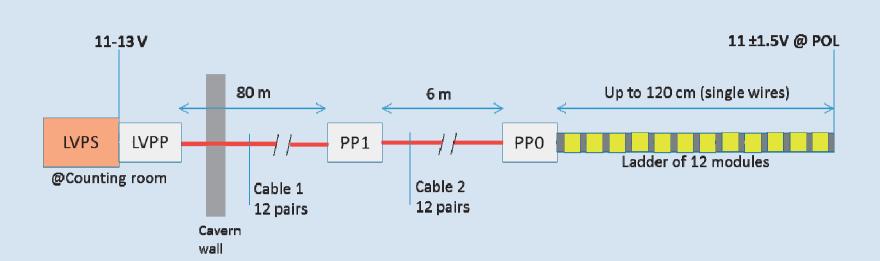
#### CMS tracker upgrade use-case

In order to be as representative as possible of the environmental conditions and technical constraints present in an HL-LHC detector, the CMS tracker upgrade is considered as a typical use-case. The upgraded CMS tracker consists of a total of 13'300 modules of 2 types, 2S and PS modules, grouped in different sub-structures depending on location. The baseline assumption for the LV distribution proof of concept is a module ladder structure of 12 PS modules. Each module uses one POL DC-DC converter.

#### **Assumption summary:**

- Monitoring and control granularity (LVPP): individual modules
- 12 PS modules / ladder
- Current consumption: 0.7A / module; 8.4A / ladder
- Targeted voltage @DC-DC: 11V +/- 1.5V
- Maximum tolerated input voltage @DC-DC: 13V
- Worst case cable length: 88 m
- Maximum voltage drop from LVPS to furthest DC-DC: 3V Cable construction: 12 individual LV feeds (divided @PP2)
- 1 LVPS channel / ladder

# CMS tracker phase II upgrade use-case and test setup



CMS tk upgrade powering baseline assumption

#### Tested equipment and setup

The technical requirement for the generic power system is divided into three categories, the AC-DC power supply (LVPS), the low voltage patch panel (LVPP or active patch panel) and the cabling. The LVPP consists of an active distribution patch panel allowing to remotely monitor the output current and control (ON/OFF) each of its output channel individually.

The cabling has been treated as part of the CMS tracker use-case and not as a generic part of the powering system.

A test PCB receiving up to 12 FEASTMP DC-DC converters has been produced.

The measurement equipment consists of a set of electronic loads to emulate the frontend chip power dissipation and an oscilloscope with current probes.

Selected and tested power supplies

- Adapted Caen A1513 (with LDR)
- Modified Wiener MPOD 0MPV8016 (with CLC) UniPower PFE3000-12 (commercial bulk power supply)
- Goessen 33K7 lab PS (commercial lab power supply)

LDR, CLC: Are both specific output voltage regulation modes made to compensate the cable Vdrop based on the PS output current.

#### **Prototype cables**

- Proto cables from Habia (12 LV pairs and 13 HV wires)
- Divided in three sections of 80m, 6m and 1.2m (last two sections in CCA wires to reduce material budget)

#### **Tested LVPP candidate (IC)**

• TI LM25066: PM bus Pwr management and protection





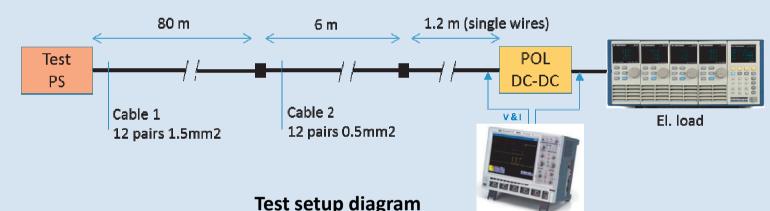


Test setup with proto cables

Tested power supply units and modules

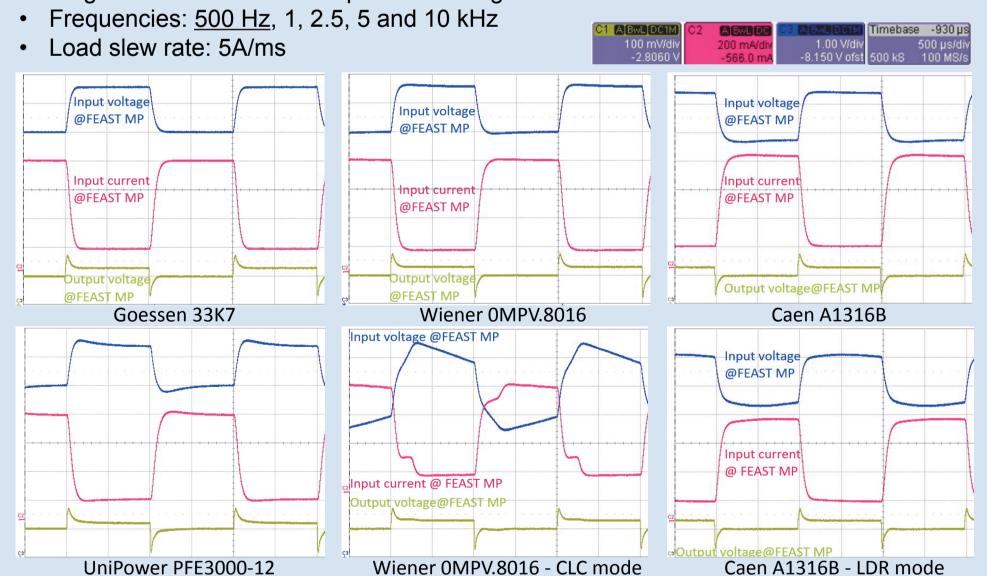
## Measurements: Various power supplies - long distance cable

The goal of the first measurements was to understand the impact on the POL DC-DC input and output voltages of the long distance cabling (almost 90m) with different power sources as well as the proposed LDR and CLC regulation modes of the custom power supplies from Caen and Wiener.



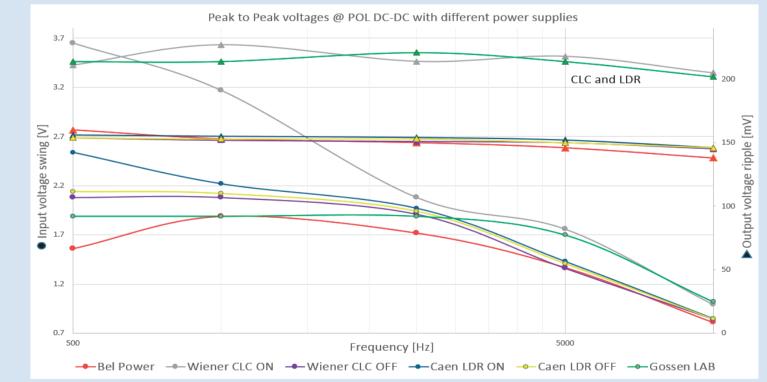
# **Test conditions:**

- 4 different PS with full proto cable chain
- Single DC-DC converter output 2.5V swing from 0.5 to 2.5A



Outcome: The POL DC-DC regulates its output very nicely despite the relatively important input voltage swing (above 3V worst case) with some LVPS

# Power sources voltage swing and effect on DC-DC output ripple comparison:



# **Specific regulation modes:**

With an important slew rate at the load (DC-DC output), both output current based regulation modes (CLC and LDR) are not fast enough to compensate the fast current variations. The regulation time constant is measured to be 2 and 4 ms respectively for Wiener CLC and Caen LDR.

# Potential gain in efficiency:

ctronics

E/e

Workshop

pical

It is shown that the special regulation modes is not fast enough to compensate the cable voltage drop in the powering scheme being investigated. However, in certain powering systems and/or applications compensating the voltage drop can have some impact on the overall efficiency of the powering chain. In the use-case being considered here this impact would however be limited to a few percents over the entire power chain. Further measurements at low frequencies are required in order to confirm the efficiency gain of such a voltage drop compensation at the power supply.

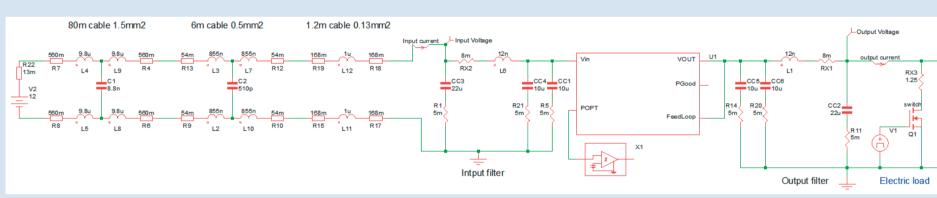
limitations (cable length) and/or with appropriate compensations (filtering important current slew rate at the load).

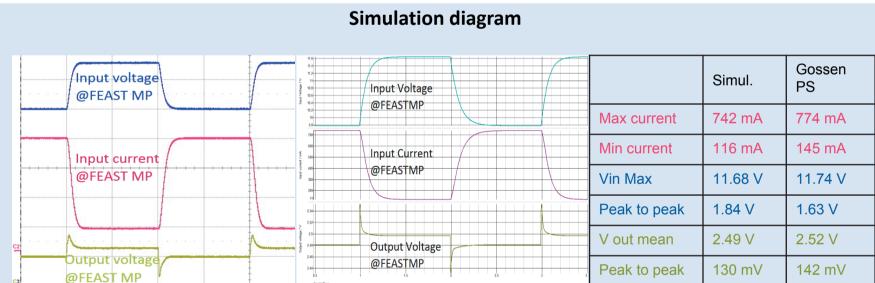
## Measurement and simulation results

#### Simulation results and proto cables

#### Simulation results:

The powering scheme was simulated using the same software used to model the POL DC-DC during its design to benefit from an existing and precise converter model. A representative load, power source and cable model was used in order to compare measured results with simulation.



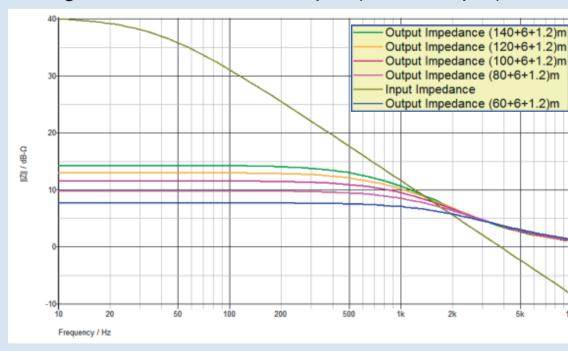


Measurement (Lab PS) Simulation The results are matching relatively well once the value of a capacitor of the POL DC-DC

input Pi filter was adapted to include its DC voltage derating (from 22 to 11uF).

# System impedance:

Once satisfying results are obtained from the simulation model, further investigations can be performed. The simulation tool offers the possibility to trace Bode plots of the impedances allowing to understand the possible impedance mismatch between the PS and the full cable length and the converter input (Pi filter input).



Impedances of converter input and various cable outputs

Independently from the different cable lengths simulated, an impedance mismatch is seen slightly above 1 kHz between the power source after the long cables and the converter input Pi filter. This impedance mismatch could potentially lead to resonating oscillations of the powering system. However, measurements shows that the POL DC-DC with its input and output filters flatten all current oscillations above this frequency.

# Cable parameters and margin:

inductance below 1 uH/m.

The cable parameters given by the manufacturer were verified using an LCR meter. The measurement results as well as the outcome of the simulation based on these

**Conclusion** 

numbers show coherent results as seen above. Different cable lengths and inductance values are simulated and lengths of 80 and 140 meters measured using the same setup as for the PS test. Simulation results with a cable of 80m show no

Measurements with cable 1 extended to 140m show good results for the supply of a single POL DC-DC converter with an input swing of 3.6V and a max. voltage below 13V.

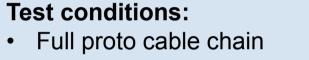
voltage overshoot with a cable

**Cable manufacturer data** Inductance Inductance (1kHz) 14 Ohms/km | 110 nF/km | 0,49 μH/m | 0,32 μH/m 1,5mm<sup>2</sup>: 0,57 μH/m 0,42 μH/m 85 nF/km 18 Ohms/km Input Voltage (0.7 uH/m inductive cable)
Maximum=11.976112V @6.1113627mSecs
Input Voltage (1.05 uH/m inductive cable) Maximum=12.302397V @4.3932747mSecs Vin simulation results with 80m cable of various inductances

## Cable cross-talk:

In order to get a feeling for the cable cross-talk between the LV pairs, a very simple measurement was preformed using the electronic loads. Lacking a setup for multiple DC-DC converters at the time of measurement, the input impedance of the load is the one of the BK precision el. load.

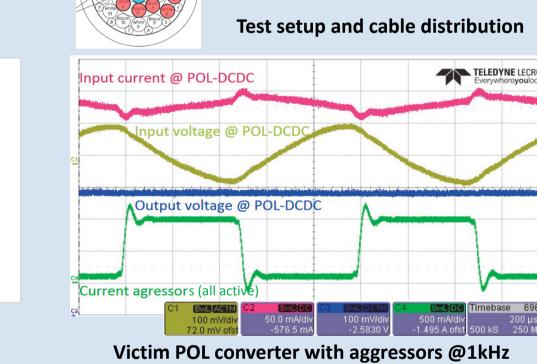
12 pairs 1.5mm2



- Victim pair @800mA DC current • El. load current swing from 0.1 to 1A on
- aggressor pairs
- Frequencies: 500 Hz, 1, 5 and 10 kHz



Victim P2P current (mA)



12 pairs 0.5mm2

Aggressor

The results show limited crosstalk up to 5 kHz. At 10 kHz and above an increase of the current swing of the victim is seen as expected from the rise of the wire inductance with frequency.

The measurement with the POL DC-DC shows that the input filter smoothes out the peaks induced by adjacent aggressors. It also illustrates that the crosstalk has almost no effect on the output voltage of the converter.

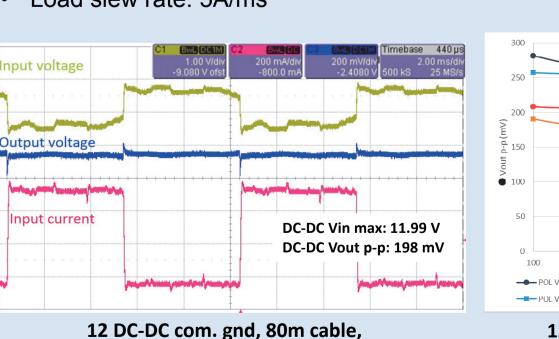
# Test results with 12 POL converters

A dedicated test pad was produced in order to be able to operate a set of 12 POL DC-DC converters in parallel in a way similar to the future CMS TK ladder of 12 PS modules. The test PCB allows connecting the LV return path to a common ground or to leave them floating.

A set of measurements was preformed using this setup with and without common ground at the POL DC-DCs.

# **Test conditions:**

- UniPower PFE3000-12 (commercial bulk power supply)
- Full proto cable chain (80+6m and 140+6m) • 12 DC-DC converters; output 2.5V swing from 0.5 to 2.5A
- Load slew rate: 5A/ms



100Hz load out of phase

12 DC-DC common gnd, 140m cable,

12 converters test pad

loads in and out of phase

The measurement results for 12 DC-DC with common ground over 80+6m of cables with the load channels out of phase, show that the output voltage swing remains acceptable, within 200mV, despite the relatively important input voltage span of up to

With an increased cable length of 140+6m and while varying the load frequency from 100Hz to 10kHz, the results are similar when the load channels are out of phase. However, synchronizing the load channels to switch in phase has an important impact on the powering system. In this case, the DC-DC output rises over 280 mV peak-topeak with a load switching at 100Hz. Similarly, with 80+6m of cable length, the output voltage PTP goes above 260mV.

# **Proof of concept**

The results contribute in building confidence that a powering scheme where the low voltage power sources are relocated in a service cavern can be envisaged, thanks to the well operating POL DC-DC converter and to the quite low inductive cable prototypes that have been procured for this project. The test of a selection of various power supply types has shown that the use of specific regulation modes is not necessarily needed and can in certain circumstances

even worsen the voltage stability at the converter input. However, for certain applications or with specific constraints (e.g. cabling), the use of a compensated PS could help ensuring the POL converter to operate at an ideal input voltage (to gain in efficiency or ensure a controlled cable Vdrop). The results also show that some PS parameters (output ripple and regulation precision) can slightly be relaxed. The measurements with 12 converters in parallel with common ground show that the specific scheme envisaged by the CMS TK upgrade is operating with certain

# Recommendations

Based on the project results and with the powering scheme considered, a few key points can be

- Standard regulated PS should be preferred (other reg. modes can present some oscillation risks)
- The wire inductance should ideally remain below 1uH/m
- Depending on the maximum tolerable DC-DC output ripple, for long cable lengths (above 80m) and/or inductance (typically above 1uH/m), load current slew rate should be limited (e.g. by additional point of load filters).