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ATLAS ITk Short-Strip Stave Prototype Module with Integrated DCDC Powering and Control

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The prototype Barrel module design, for the Phase II upgrade of the of the new Inner Tracker (ITk) detector at the LHC, has adopted an integrated low mass assembly featuring single-sided flexible circuits, with readout ASICs, glued to the silicon strip sensor. Further integration has been achieved by the attachment of module DCDC powering, HV sensor biasing switch and autonomous monitoring and control to the sensor. This low mass, integrated module approach benefits further in a reduced width stave structure to which the modules are attached. The results of preliminary electrical tests of such an integrated module will be presented.

Summary

The Phase II upgrade of the ITk detector at the LHC requires the modules to have high density channel counts whilst also maintaining minimal material to ensure their optimum performance within a tracking environment. For the ATLAS ITk Short-Strip Stave Module, material reduction has been achieved by a multifaceted approach. The front-end readout ASIC count has been reduced by a factor of two, compared to previous prototype versions, by the scaling up of the number of channels from 128 to 256; this has been realised in the ABC130 ASIC fabricated in 130nm CMOS technology. The readout ASICs are then attached to a low mass single-sided flexible circuit, of minimal width, whose layer count has been reduced by adopting an asymmetric circuit stack-up; with the power supply Ground plane on the bottom (which is referenced to the sensor), removing the requirement for a dedicated shield layer. Test results showing that digital pickup into the sensor is only evident at front-end comparator thresholds well below the nominal setting for normal operation.
Due to geometrical constraints, the module powering, HV sensor switching and control have also been attached to the silicon strip sensor. The integration of front-end readout ASICs and their carriers plus powering, switchable sensor biasing and autonomous monitoring and control results in a compact, self-contained module topology. This is beneficial for the stave structure, to which the modules are attached, as the stave width can be further reduced due to the module powering and control being no longer required to reside on the stave as initially proposed. The integration of module powering, HV sensor switching and control ASIC has been realised by the development of a separate power board. A novel feature of the powering block is the use of a DCDC buck converter, based on the CERN FEAST2 ASIC. Due to the nature of their operation, buck converters can have large EMI emissions which can produce induced noise into both the silicon strip sensor and front-end readout ASIC. Limitations in both height and width make it non-trivial to fit a toroidal coil of the nominal inductance, this would be the preferred choice of coil due to its low EMI; instead a solenoid type was chosen. The adoption of a low mass, mixed material (Al/Cu), shielding solution has been shown to work very well in the attenuation of EMI whilst still maintaining a target efficiency of 75% at the nominal load of 2A.
Prototype modules and power boards have been constructed and shown to work very well, with the integrated module performance meeting the module design specification.

The work is relevant to the power topic. The conclusion is that with correct design it is possible to obtain good low noise performance of silicon detector modules using DCDC converters even when located in close proximity to both silicon sensor and sensitive front-end electronics.

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