Contribution ID: **141** Type: **Poster**

The Quality Assurance of a Low-Latency, Low-Overhead, Dual-Channel Transmitter ASIC for the ATLAS Liquid Argon Calorimeter Phase-I Upgrade

Tuesday 12 September 2017 17:00 (15 minutes)

We present the quality assurance (QA) test of LOCx2, a low-latency, low-overhead transmitter ASIC for the ATLAS Liquid Argon Calorimeter Phase-I upgrade. In the QA test we will screen about 7000 LOCx2 chips to ensure their basic functionality. The QA test system, including two printed circuit boards, firmware, software, are under development. All tests are automatically conducted and controlled by LabVEW software running on a computer. The test results will be reported.

Summary

The ATLAS Liquid Argon Calorimeter (LAr) Phase-I trigger upgrade requires high-speed, low-latency data transmission to read out the LAr Trigger Digitizer Board (LTDB). To meet this requirement, LOCx2, a dual-channel transmitter ASIC, has been designed, each channel operating at 5.12 Gbps. LOCx2 can accommodate data from three types of ADCs, an ASIC ADC and two Commercial-Off-The-Shelf (COTS) ADCs. About 7000 LOCx2 chips have been produced and are in packaging process. In order to ensure the basic function of the chips before assembly, a Quality Assurance (QA) test must be conducted.

The QA test measures the serial output eye diagram, the Bit Error Rate (BER) and the I2C interface of each chip. We also plan to sample about 1% of the chips that pass the above tests in each wafer to measure the Phase-Locked-loop (PLL) tuning range, the jitter of the serial output, and check the 3.125-ns skew tolerance in the ASIC ADC mode.

The QA test system has two setups. The first setup is for eye diagram observation, the PLL tuning range tests and serial output jitter measurement. The eye diagram, the PLL tuning range, and the serial output jitter are measured by using a high-speed real-time oscilloscope. The eye diagram and the serial output jitter are observed on the 5.12-Gbps serial output signals. The PLL tuning range is measured on the PLL output signal when the input clock frequency is adjusted. The printed circuit board (PCB) used to characterize the chip before will be used in the test. To shorten the test, LabVIEW will be used to control automatically the procedure and record the test results.

The second setup is for the I2C interface, the BER, and input skew tests. The BER test will be measured under the combination of three different power supply voltages (2.25 V, 2.5 V, 2.75V) and three ADC types. The BER test is the most time-consuming part. In order to shorten the BER test time, a QA test system is being developed so that six chips are tested simultaneously. The system includes a commercial FPGA evaluation board KC705, two printed circuit boards (PCBs), FPGA firmware, and software written in LabVIEW to control the system. KC705 is used in the system as ADC data generators and the data link receivers with error loggers. Since the KC705 does not have enough pins to output ADC signals to six chips, only one ADC emulator is implemented in the FPGA. Two test PCBs are being developed. The ADC emulator signals from the FPGA are fanned out into six groups on the first PCB. Twelve pairs of differential high-speed signals from six chips are output to the FPGA, four pairs via the first PCB and the other eight pairs via the second PCB and coaxial cables. In order to test the BER automatically, software is developed in LabVIEW to control the test process.

All the 7000 LOCx2 chips will be tested in this summer. The QA test result will be presented in the workshop and the proceeding.

Authors: Dr XIAO, Le (Department of Physics, Central China Normal University, Wuhan, Hubei 430079, P.R. China); LIU, Chonghan (Southern Methodist University); Dr ZHAO, Xiandong (Southern Methodist University); Dr DENG, Binwei (Hubei Polytechnic University); Dr GONG, Datao (Department of Physics, Southern Methodist University, Dallas, TX 75275, USA); GUO, Di (University of Science and Technology of China); Ms HE, Huiqin (Shenzhen Polytechnic); HOU, Suen (Academia Sinica (TW)); LIU, Tiankuan (Southern Methodist University (US)); Dr SUN, Quan (Department of Physics, Southern Methodist University, Dallas, TX 75275, USA); WANG, Jian (Univ. of Sci. & Tech. of China); XIANG, annie (Southern Methodist University); Mr YANG, Dongxu (Department of Physics, Southern Methodist University, Dallas, TX 75275, USA); YE, Jingbo (Southern Methodist University, Department of Physics); Mr ZHOU, Wei (Department of Physics, Central China Normal University, Wuhan, Hubei 430079, P.R. China)

Presenter: LIU, Tiankuan (Southern Methodist University (US))

Session Classification: POSTER Session

Track Classification: Production, Testing and Reliability