Contribution ID: **133**

Type: **Poster**

Electrical and Functional Characterisation with Single Chips and Module Prototypes of the 1.2 Gb/s Serial Data Link of the Monolithic Active Pixel Sensor for the Upgrade of the ALICE Inner Tracking System.

Tuesday, 12 September 2017 16:45 (15 minutes)

The upgrade of the ALICE Inner Tracking System uses a newly developed Monolithic Active Pixel Sensor (ALPIDE) which will populate 7 tracking layers surrounding the interaction point. Chips communicate with the readout electronics using a 1.2 Gb/s data link and a 40 Mb/s control link. Event data are transmitted to the readout electronics over microstrips on a Flexible Printed Circuit and a 5m long twinaxial cable.

This contribution describes the experimental characterisation activity to verify the reliability of control and data transmission for single chips and prototypes of the detector modules, in laboratory setups and beam tests.

Summary

The upgrade of the ALICE Inner Tracking System uses about 25000 specifically developed, large area Monolithic Active Pixel Sensors (MAPS), arranged in 7 cylindrical layers surrounding the interaction point. Each layer is segmented into staves. In the 3 innermost layers, a stave contains 9 sensors. Each sensor sends data directly to the readout electronics over a dedicated data link. The 4 outer layers segment staves into half-staves and modules, with one half-stave built out of 4 or 7 modules. One module combines 14 sensors in a master/slave configuration, with two master chips controlling 6 slave chips each. Every master chip has a data link to the readout electronics. Slave data is forwarded on a local bus to the master chip. The operating bit rate for the data links is 1.2 Gb/s for the three inner layers and 400 Mb/s for the four outer layers. The physical medium includes microstrip traces on the Flexible Printed Circuits and a 5 m long twin, mini-coaxial cable to the readout electronics.

The pixel sensor used is a custom designed chip named ALPIDE, fabricated in an 180 nm CMOS process. It uses a custom Data Transmission Unit (DTU), combining a Phased Locked Loop (PLL), a Double Data Rate (DDR) serialiser and a pseudo Low-Voltage Differential Signalling (LVDS) driver with pre-emphasis.

This contribution outlines the characterisation effort for assessing the DTU performance of single sensors and prototypes of the detector modules. Laboratory test setups were designed to model the final system as close as possible. The test setups use the same electrical transmission line as planned for the final system. The receiver links on the readout electronics side were implemented using the first prototype of the final readout system. Testing procedures to assess electrical, functional and jitter performance were implemented using the different prototypes of single sensors and modules. An electrical characterisation of the transmission lines for both control and data link was performed. A jitter study of the data link describes the jitter behaviour in relation to chip load and supply noise. The results were compared with the previous chip prototypes to check the improvements of the modifications made in the circuits. This study provided input to establish the operating conditions and margins for reliable transmission of data.

An irradiation campaign was performed, testing the chip and in particular the Data Transmission Unit under radiation in a 30 MeV proton beam. The behaviour of the DTU's components was monitored during the tests, analysing signs of upsets or functional interrupts of the circuitry. Received bit sequences were checked online for bit errors, event data from test pulses collected for offline analysis. No functional or data upset was observed during irradiation. There was no observation of an increase of jitter due to irradiation.

This contribution will describe the setup, the characterisation techniques and the experimental results, focusing on the electrical and jitter performance. It will include results from the irradiation tests.

Primary authors: LUPI, Matteo (Johann-Wolfgang-Goethe Univ. (DE)); BONORA, Matthias (University of Salzburg (AT)); AGLIERI RINELLA, Gianluca (CERN)

Co-authors: Mr DAEHYEOK, Kim (Yonsei University); KUGATHASAN, Thanushan (CERN); LATTUCA, Alessandra (Universita e INFN Torino (IT)); MAZZA, Gianni (Universita e INFN Torino (IT)); SIELEWICZ, Krzysztof Marek (Warsaw University of Technology (PL)); SNOEYS, Walter (CERN)

Presenter: BONORA, Matthias (University of Salzburg (AT))

Session Classification: POSTER Session

Track Classification: Production, Testing and Reliability