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The Quality Assurance Test of a VCSEL Driver ASIC for the ATLAS Liquid Argon Calorimeter Phase-I Upgrade

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A VCSEL driver ASIC, LOCld, has been designed for the ATLAS Liquid Argon Calorimeter Phase-I Upgrade. In total about 7000 chips have been produced and are in packaging process. We present the quality assurance test aiming at screening all functional chips before they are assembled into optical transmitter modules. A detailed test procedure is proposed. A dedicated test board has been designed and in fabrication. The test results will be present in the workshop and in the proceeding.

Summary

LOCld is a dual-channel vertical-cavity surface-emitting laser (VCSEL) driver ASIC designed for the optical data link to read out the ATLAS Liquid Argon Calorimeter. LOCld will be assembled in MTx, a dual-channel optical transmitter module and in MTRx, an optical transceiver module. In MTx each channel of LOCld operates at 5.12 Gbps. In MTRx, only one channel of LOCld operates at 4.8 Gbps and the other channel is not powered up. In total about 7000 LOCld chips have been produced and are in packaging process. In order to ensure the functionality of LOCld and save the production cost of MTx/MTRx, a quality assurance (QA) test will be conducted on each LOCld chip. Only the chips passing the QA test will be assembled in MTx or MTRx.

A detailed QA test procedure is proposed. The QA test includes an I2C configuration test, an eye mask test, the bias current range, and a bit-error-rate (BER) test. Firstly, for the I2C test, we use the I2C interface to read the internal registers of each chip after power-up and write the registers and read back the configuration registers. Secondly, a custom eye mask at 5.12 Gbps is used to screen the eye diagram of each the ASIC. The modulation current is set to an optimal value estimated from the prototypes. The power consumption will be recorded. Those chips with power consumption beyond three times of standard deviation away from the average value will be discarded. Thirdly, the minimum and maximum of the bias current of LOCld will be measured. Finally, about 1% of the chips from each wafer will be put in a BER test for 15 minutes.

A dedicated test board has been designed and is in fabrication process. Four channels of two chips will be tested at the same time with a single test board. Each chip is placed in a socket. The single-channel signal in a pattern of a pseudo-random binary sequence 2^7-1 from a signal generator of a bit error rate tester will be fanned out to two chips under test. The output signals of each chip will be connected to differential probes of a high-speed real-time oscilloscope.

The QA test is planned in June and July of 2017. The test results will be presented in the workshop and in the proceeding.

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