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A Multi-Channel PCI Express Readout Board Proposal for the Pixel Upgrade at LHC

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After having commissioned the readout electronics currently implemented in the Insertable B-Layer, Layer 1 and Layer 2 of the ATLAS Pixel Detector (B-Layer and Disk readout electronics in under commissioning), we have designed and fabricated a new readout electronic board looking at the upgrade of the LHC pixel detectors. A couple of PCI_express-based prototype boards, namely PCI-ROD featuring all the minimal I/Os and interfaces to address the future front-end electronics, have already been fabricated and tested. The GBTx and RD53A are the first chips that we are going to interface with: preliminary tests are here presented.

Summary

Over the last years the ATLAS Pixel Detector has been upgraded in terms of sensors and readout electronics. The sensors, the back-of-crate and readout-driver cards have been upgraded for the Insertable B-Layer, while the Layers 1 and 2 have maintained the current sensors and have updated only the readout electronics to stand the on-going increment of luminosity of the collider at CERN. All these layers have already token data while the readout electronics upgrade for the B-Layer and Disks is under commissioning and it will be completed in the technical stop of 2018. To continue the challenge of upgrading the readout electronics for the LHC pixel detectors we have designed and fabricated a PCI_express 8-channel board (PCI-ROD) with all the necessary I/Os looking at the performance to interface with the current and future front end electronics chains. For example, the intention is to interface with the GBTx and RD53A chips.
In particular the GBTx communication has already been tested via an optical transceiver at a speed of 10 Gb/s in a loopback configuration. In addition, a board designed for the ALICE time-of-flight experiment, mounting a GBTx ASIC, has been physically interfaced with the PCI-ROD through an optical fiber at a speed of 4.8 GB/s.
As far as the RD53A chip interface, we are building a demonstrator tool able to emulate a data-taking of physical streams, using the Aurora protocol, by connecting two PCI-ROD boards. One is used to build the expected RD53A emulated data and the other one is the receiver. This can be run at data rates up to 10 Gb/s on a single channel or in parallel over several links.
The PCI-ROD board features two Xilinx FPGAs: the Kintex7 XC7K325T-2FFG900C and the Zynq XC7Z020-1CLG484C with an embedded physical dual-core ARM Cortex-A9 processor. The Kintex device allows 16 transceivers nominally running at up to 12 Gs/s. These 16 GTx are connected to different types of physical ports: 8 PCI_express, 4 HPC FMC, 1 LPC HMC, 1 SMA, 1 SFP and 1 Gb-Ethernet port. So far we have proved the coaxial link to the SMA, the optical channel to the SFP and the Ethernet links up to 10 Gb/s.
In addition the two Xilinx devices feature DDR3 external memories tested with read-write cycles at 667 MHz.

The PCI-ROD board can be equipped with a firmware derived from the one that is currently working into the BOC and ROD boards of the ATLAS Pixel Detector.
As the PCI-ROD features 16 GTx channels we are proposing the board as a tool to test, qualify and read out the recent chips and/or channels under development to interface the new generation of the Pixel Detectors at LHC. We start working within the ATLAS ITK italian collaboration to help qualifying some the RD53A modules expected by this year. We are also planning extend the use of the board within other CERN-based collaborations.

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