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A SEU-Immune Self-Tuned Pixel Chip Architecture

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Readout chips of hybrid Pixel detectors use low power amplifier and threshold discrimination to sense and digitise charge deposited in semiconductor sensor. Due to variability in CMOS transistors each pixel circuit needs to be calibrated individually to achieve response uniformity. Traditionally this is addressed by programmable threshold trimming in each pixel. In this presentation a self-adjusting threshold mechanism is presented, which corrects the threshold for both spacial and time variation. The behaviour of this circuit has been simulated to evaluate its performance compared to traditional calibration results. The simulation results show that this mechanism can perform equally well, but eliminates instability over time and is immune to single event upsets.

Summary

The self-adjusting mechanism exploits the electrical noise as relative measure for the threshold and automatically adjusts the threshold to always achieve the same frequency of noise hits passing the threshold. The mechanism is implemented in form of an up/down counter and combinatorial filter logic, which replaces the traditional trim DAC register. This circuit could be a key technology to enable smooth detector operation in HL-LHC conditions, as it mitigates a variation in pixel threshold cause by Single-Event-Upsets of digital logic and changing transistor characteristics resulting from change in temperature or induced by ionising radiation.

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