Contribution ID: **106** Type: **Poster**

The End-Of-Substructure Card for the ATLAS ITk Strip Tracker

Wednesday, 13 September 2017 16:45 (15 minutes)

The End-Of-Substructure Card (EoS) is the interface between the building block of the ITk Strip Tracker and the outside world. All the control and command signals, the data and the power will be passing through it. The card concept is built around using the lpGBT chip set and the VTRx optical link. The EoS will handle up to 28 640 MBit data links and 10 GBit Downlinks and Uplinks. It will be powered using a two-stage DCDC converter system. A first prototype was developed using the GBTx chipset, supporting link speeds up to 5 Gbit. We present first performance measurements of the system including the performance of the DCDC system.

Summary

The End-Of-Substructure Card (EoS) is the interface between the building block of the ITk Strip Tracker (staves and petals) and the outside world. In the ITk the modules consisting of the silicon sensor itself and the hybrids with the readout ASICS are placed on a common structure called a stave (in the barrel) and petal (in the end-cap). All module use a common bus-tape co-cured to carbon-fiber based structure to distribute power and signals. The data lines and command lines are then connected from the bus-tape to EoS. The power, both low and high voltage, are also distributed via the bus tape and coonected to the EoS. All these connections will be made using wire-bonds. The card concept is build around using the lpGBT chip set and the VTRx optical link, both common developments for the LHC Upgrades. The command signals will be coming in on a 10 Gbit/s link and will be de-multiplexed by the lpGBt and send to the stave/petal. The incoming data from the sensor, which depending on the type of stave or petal will be up to 28 lines, will be at a rate of 640 Mbit/s and be then multiplexed by one or two lpGBTs into 10 Gbit/s data links. The conversion from electrical to/from optical will be handled by the Vtrplus chips set. All the power lines including sense wires will be going through the EoS. The LV lines will be rated for 12 V and the HV lines for 750 volts. The EoS itself will be powered using the 12 V and generate 2.5 and 1.2 V using a DCDC converter system using the upFeast and DCDC2s chips currently developed at CERN.
As a first prototype for the Stave2017 program an EoS has been designed and manufactured using the GBTx/VTRx chipset, which supports link speeds up to 5 Gbit. We present first performance measurements of the system including the performance of the DCDC system.

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Session Classification: POSTER Session

Track Classification: Radiation Tolerant Components and Systems