SOLAR

A SAMPA to Optical Link for ALICE Readout card

A. Grabas, D. Besin, C. Flouzat, B. Paul,

IRFU, CEA, Université Paris-Saclay, F-91191, Gif-sur-Yvette, France

Introduction and System Architecture

CONTEXT

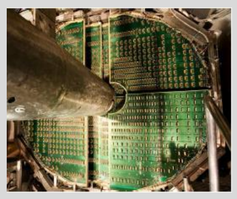
LS2 global upgrade (2019 – 2020)

- Pb-Pb collisions at up to L=6.1027 $cm^{-2}s^{-1}$
  - **Hadronic Interaction Rate = 50kHzLHC** → **Factor 2 safety margin : Readout at 100 kHz**
  - **On detector rad hard electronic**
- ALICE Goal: Integration of 13 nb^{-1} for Pb-Pb collisions
  - **Very small signal to background ratio** → **Dead time free data readout**

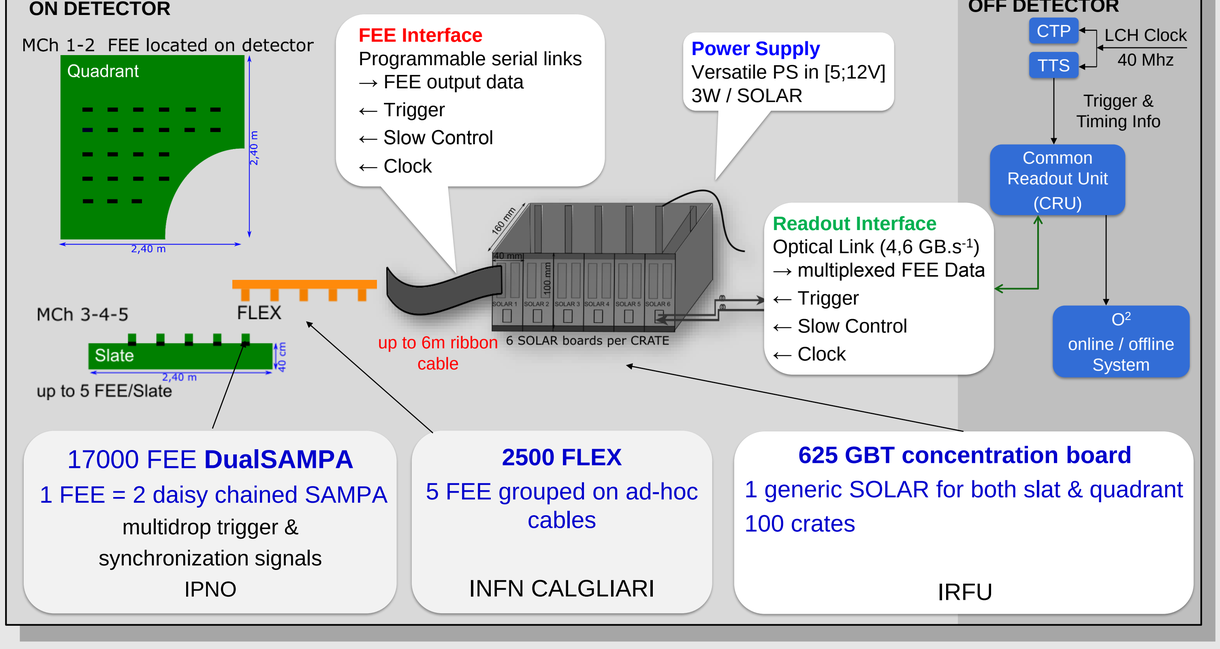
New ALICE Readout Electronics

ALICE Muon Tracking Chambers

- 156 multi-wire proportional chambers → **Same Detector implementation**
  - → Cathode Pad Readout
  - → More than 1 million channels → **34000 On detector SAMPA Asics (32 channels)**
  - → Spatial Resolution > 100µm
  - → Max input signal: 500fC
  - → Gain: 4mV/fC
- System of 5 Tracking Stations (TS), 2 chambers each
  - → **2 Designs**: 16 Quadrants (TS1,2) & 140 Slats (TS 3,4,5)
- Radiation: TID < 1krad - Fluence < 4.10^{11} n 1 MeV equivalent
- Magnetic Field: 0.7 T



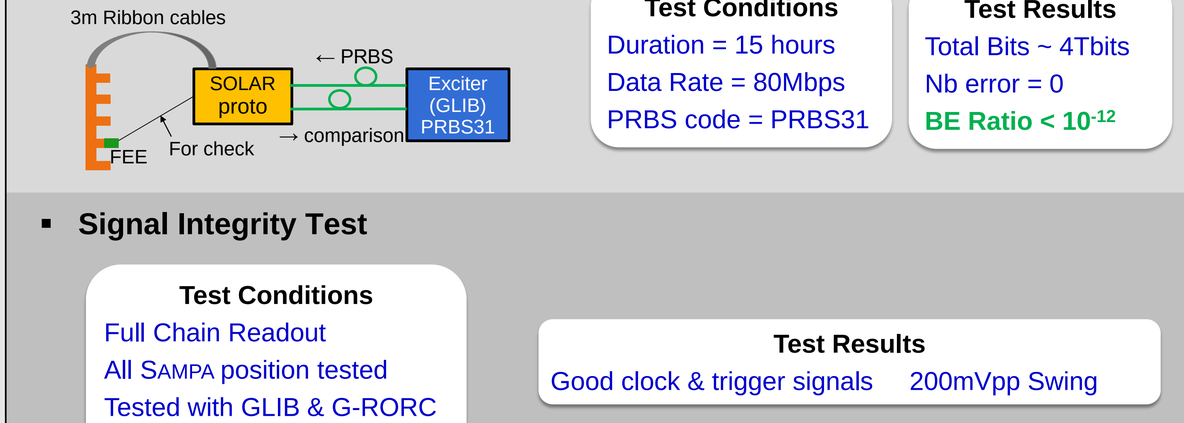
Upgraded ALICE Muon Chambers Readout Electronics



DESIGN of the SOLAR Concentration board

SOLAR FUNCTIONAL BLOCK DIAGRAM

a SAMPA to Optical Link for ALICE Readout

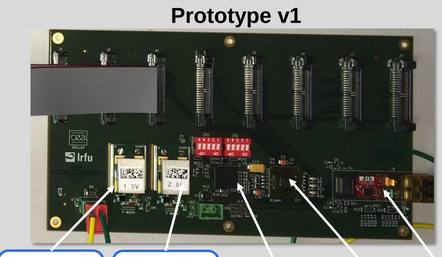


4 multidrop triggers with up to 5 FEE

- → Hard Reset: Reset all FEE Registers
- → Physics Trigger
- → Heartbeat: Synchronization
- → Bunch Crossing Counter Reset

***CERN COMPONENTS**
GBT, Versatile Link, and FEASTMP Family

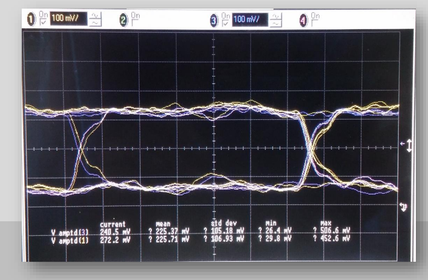
Prototype v1



SOLAR SPECIFICATIONS

Thanks to GBT family + Versatile Link + FEASTMP DCDC CERN components

- **BROADCAST clock and trigger toward up to 40 FEE**
  - 32 multidrop SLVS output at 80 Mbit.s^{-1} (Trigger)
  - 40 point to point SLVS output at 80 Mbit.s^{-1} (Clock)
- **CONCENTRATE data from up to 40 FEE**
  - 40 inputs SLVS at 80 Mbit.s^{-1}
- **CONFIGURE up to 40 FEE**
  - 8 I2C bus
- **INTERFACE with ALICE CRU**
  - 1 GBT bi-directional optical link @ 4.8 Gbit.s^{-1}
  - → To CRU : up to 40 multiplexed FEE data stream
  - → From CRU : trigger info & Clock
- **Hard Environment**
  - Rad Hard + Magnetic Tolerant Electronics
  - Mechanical constraints : 3U x 160 mm board



- **Tracking /Traceability**
  - 1 unique ID onboard
- **Power supply**
  - Versatile PS in [5, 12]V range
  - 3 W per SOLAR Board

Test and Validation

First prototype validated in Lab

- **Bit Error Test**

3m Ribbon cables

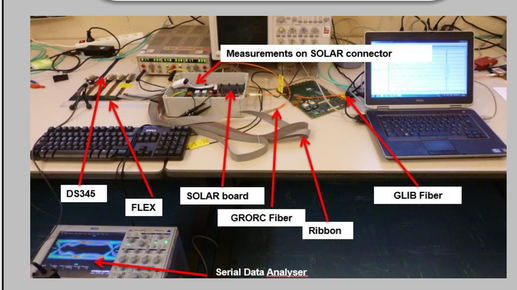
Test Conditions
- Duration = 15 hours
- Data Rate = 80Mbps
- PRBS code = PRBS31

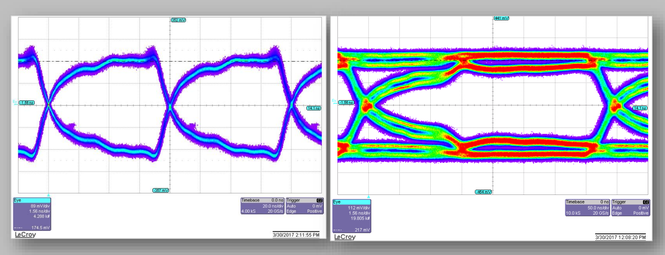
Test Results
- Total Bits ~ 4Tbits
- Nb error = 0
- **BE Ratio < 10^{-12}**

- **Signal Integrity Test**

Test Conditions
- Full Chain Readout
- All SAMPA position tested
- Tested with GLIB & G-RORC
- Trigger and Clock Signals

Test Results
- Good clock & trigger signals 200mVpp Swing





- **Validated along Beam Test at CERN using PS**

Next step: SOLAR mass production

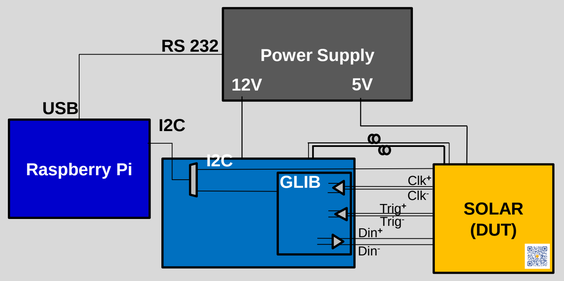
- **Functional Test Bench at the cabling house**

SOLAR Board Identification using QRcode and Unique ID

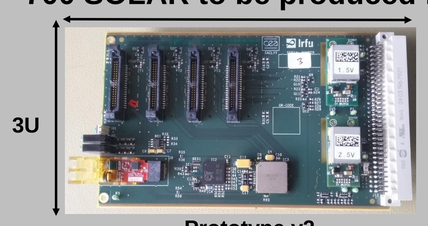
Fully automated OK / NOK functional test:
- → I2C transaction test on all I2C Bus
- → Din^+/Din^- and $Trig^+/Trig^-$ testing using checkerboard patterns
- → Clk^+/Clk^- toggling
- → Power Consumption

GBTx efuse Configuration

Traceability: store test data for all SOLAR



- **700 SOLAR to be produced by Q'4 2018**



Prototype v2

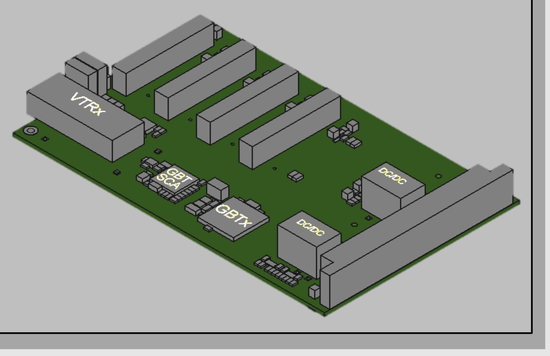
early September '17 - - Prototype v2 received at Saclay

end October '17 -·-·- Pre Serie Production Start (25 boards)

January '18 -·-·-·- Serie Production Start (675 boards)

October '18 -·-·-·-·- End of Production

Final SOLAR 3D View



christophe.flouzat@cea.fr
aude.grabas@cea.fr
bernard.paul@cea.fr