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Concentration Card Prototype SOLAR and Readout Electronics Principle for ALICE Muon Tracking Chambers Upgrade

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In the framework of the ALICE experiment upgrade at HL-LHC, the whole electronics of the existing Muon Tracking Chambers (MCH) will be refactored with a new frontend chip and the associated readout electronics. This paper presents the design of the dedicated concentration cards 'SOLAR'to ensure the readout of 30,000 frontend chips. Based on the CERN GBTx and FEAST DCDC chips, allowing to work in a radiation and magnetic field environment, each of the 650 SOLAR cards can broadcast configuration, trigger and synchronization signals and gather the data of up to 80 frontend chips through up to 6 meter cables.

Summary

In the frame of the upgrade of the LHC (Large Hadron Collider) at CERN, the existing ALICE (A Large Ion Collider Experiment) prepares a major upgrade of its experiment apparatus, planned for installation in the second long LHC shutdown (LS2) in the years 2019-2020. This will include the upgrade of the Muon Tracking Chambers (MCH), and especially the update of its electronics. This refactor involves the frontend replacement by a dedicated ASIC 'SAMPA', along with an upgrade of the readout for all the 5 tracking stations. For compatibility with the existing detector and taking into account the detector occupancy, the ˜ 30,000 SAMPA chips involved are grouped by 2 on a 'Dual-Sampa'(DS) board. The configuration and the readout of all the SAMPA chips is then ensured by ˜ 650 concentration cards 'SOLAR', and connected optically to ALICE Common Readout Unit (CRU). Taking into account the radiation (TID < 1 krad, fluence < 4.1011 n 1 MeV equivalent) and magnetic field (0.7 T) environment, the design of the SOLAR concentration board is based on the GBTx (gigabit transceiver), the GBT-SCA (slow control companion chip), VTRX (versatile transceiver) and the FEASTMP (DC/DC converter) devices developed at CERN. With regard to the granularity of the elinks in the GBTx and the integration constraints, especially keep a generic design for SOLAR with the two types of MCH stations (quadrants and slats), each SOLAR board was designed to connect to up to 40 DS cards through up to 6 meter cables. In this design, DS cards are grouped by cluster of up to 5 cards, such that each SAMPA ASIC can be configured individually, while the trigger and synchronization signals are shared by up to 10 SAMPA chips. Downstream, the 2 SAMPA chips on a DS board are daisy chained, each DS board having its dedicated 80 Mbit/s elink toward the SOLAR card. In addition to this, a chip with a unique ID was included onboard the SOLAR board to ensure board identification for traceability at the production step, but also for tracking the SOLAR boards along their life cycle in the MCH detector. With a power consumption below 3 W for a versatile power supply in the range 5 to 12 V, thanks to the FEASTMP DC/DC, first results with the first SOLAR prototype are very encouraging, even with 6 meter flat ribbon cables, allowing a full chain validation including the configuration and the readout of 5 DS cards, in a beam test at CERN. A new design, fitting into a standard 6U format crate, and a dedicated production test bench are developing for the end of 2017.

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