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Development of a Monolithic Low Power, High Speed Pixel Sensor for Particle Tracking in High Energy Physics Experiments

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We have developed a 2nd generation high resistivity CMOS process, suited for integration of complimentary pixel circuitry. High charge collection efficiency can be maintained after neutron irradiation up to 1016 neq/cm2 when applying a depletion voltage to the backside of the 50 µm thick devices. Results measured with a 15 µm MAPS detector, fabricated in this technology, will be presented.

Based on the Orthopix architecture, we are developing a megapixel detector with digital pixel output on 20 µm pitch supporting a frame rate of 50 MHz at a power dissipation of 200 mW/cm2. Process and design will be presented.

Summary

The next generation of detectors for high energy physics experiments with high luminosity must support hit rates >1 MHz/mm2 and remain functional after accumulating a neutron radiation dosage up to 2x1016 neq/cm2. In addition, the excellent tracking information of today's pixel detectors must be extended to cover a larger area while at the same time existing power budgets must not be exceeded. Present generation pixel detectors are mostly based on hybrid or 3D IC technology, but it is questionable whether they can be fabricated sufficiently economically to meet budget constraints.

Monolithic Active Pixel Sensors (MAPS), fabricated using mainstream CMOS image sensor (CIS) processes, can be operated with very low power consumption and can be produced in large quantities at low cost. However, available CIS technologies use low resistivity silicon and only allow integration of one type of transistor inside the pixel (typically NMOS). These constraints cause limitations in the maximum achievable readout speed, minimum power consumption, and radiation hardness. Some improvements in radiation hardness could be made in such devices when adding a high resistivity EPI layer, thereby introducing a drift component to the charge collection. But preferably a detector backside bias voltage can be increased as radiation damage is accumulated. This is the practice pursued in existing hybrid pixel detectors.

Sensor Creations has developed a custom CMOS process using high resistivity float zone wafers. The feasibility of this technology was demonstrated in a 640x512 pixel resolution imager with 15 µm pitch. The devices are 50 µm thick and can be fully depleted by applying a voltage of at least -10V to an electrode that is added to the backside of thinned wafer. The 1st generation devices, however, suffered from early breakdown causing high leakage current and low quantum efficiency due to incomplete depletion.

After an extensive analysis of the structure using TCAD simulation tools, the process was revised and a 2nd generation high resistivity CMOS technology created. In the improved process implementation, full depletion can be achieved without breakdown. In addition, it is now possible to integrate complementary circuitry into the unit cell so that a functionality, comparable to that of hybrid pixel detectors, can be supported.

In this presentation, we will show measurement results from our fully redesigned 640x512 pixel image sensor, processed in the 2nd generation technology. In addition, we will review on-going design work for a radiation hard, high speed low power megapixel detector array based on the "Orthopix"architecture. In the new monolithic sensor, the pixel comprises a charge amplifier and discriminator and all data transfer inside the array is done in the digital domain. The new device has a pixel pitch of 20 µm and can be read out at a frame rate of 50 MHz and a power dissipation of 200 mW/cm2. This level of performance meets the initial goal of a 1 MHz/mm2 hit rate within existing power budgets.

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