Next generation ATCA control infrastructure for the CMS Phase-2 upgrades

Aleš Svetek, Jes Tikalsky, Marcelo Vicente, Robert Fobes, Sridhara Dasu, Tom Gorski and Wesley Smith

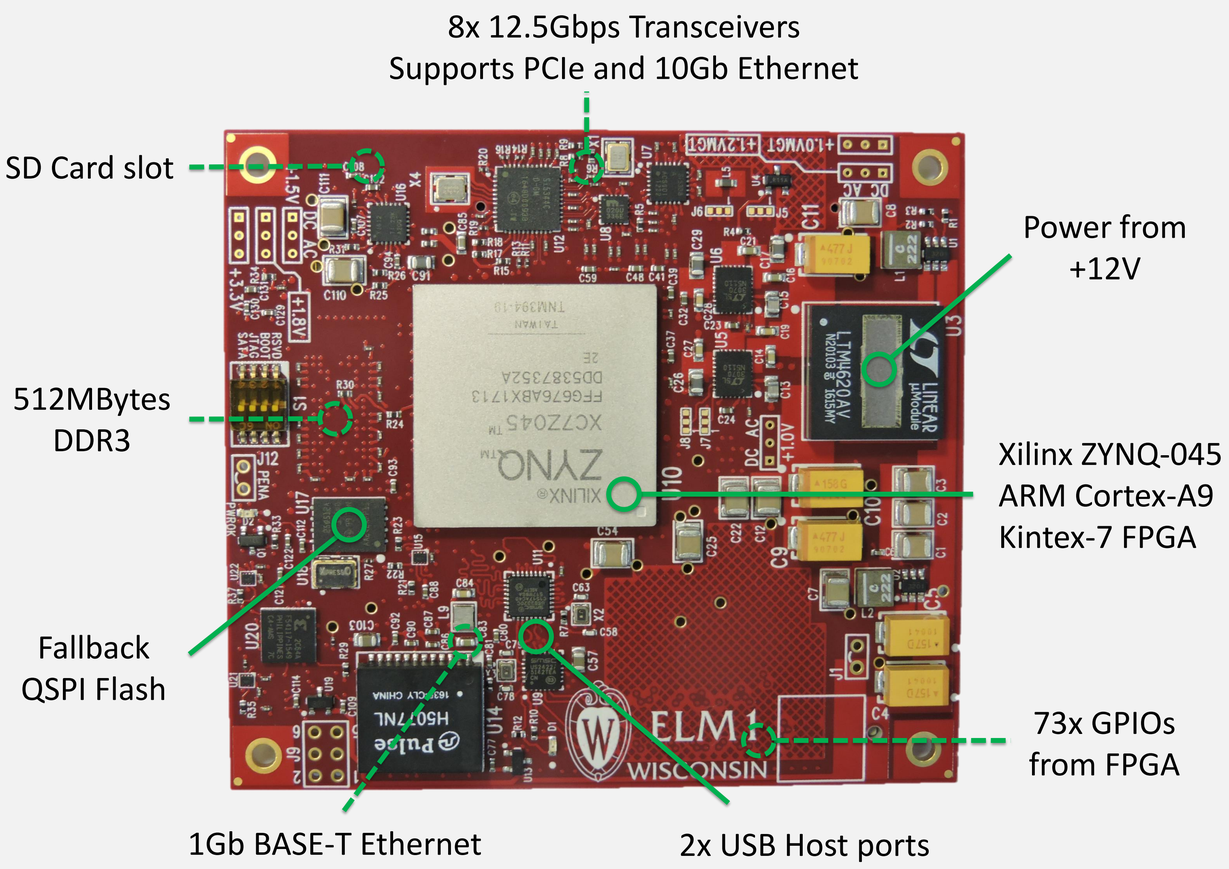
University of Wisconsin-Madison

Overview

A next generation open-source control infrastructure is being designed and tested for the CMS upgrades that will take place during the Long Shutdown 3 (LS3). Most of the architectural choices have been focused in designing AdvancedTCA (ATCA) blades and, as part of the PICMG 3.x standard, each ATCA blade needs to implement a set of control and management functionalities.

The next generation control infrastructure can be seen as a hardware and firmware evolution of existing solutions by exploiting newer technologies and programming techniques. The presented infrastructure provides better configurability, increased responsiveness and decreased development time and testing of ATCA blades.

Embedded Linux Mezzanine

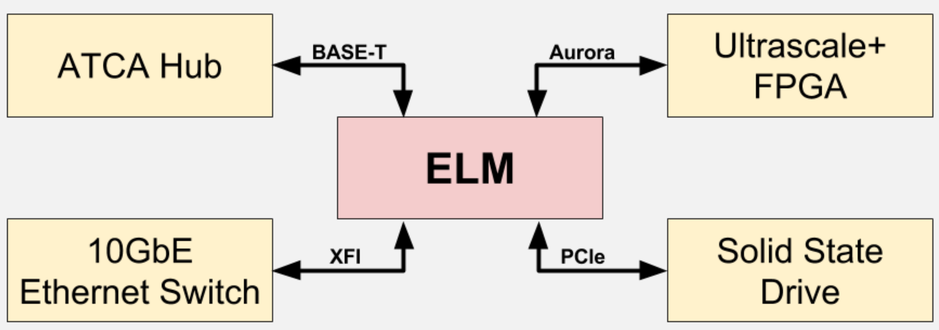


Short for ELM, the Embedded Linux Mezzanine is intended to be used as the blade's on-board computer and its primary access point. It features a dual core ARM processor packed inside a high-end Xilinx ZYNQ System-on-Chip (SoC) running a full-fledged Linux distribution.

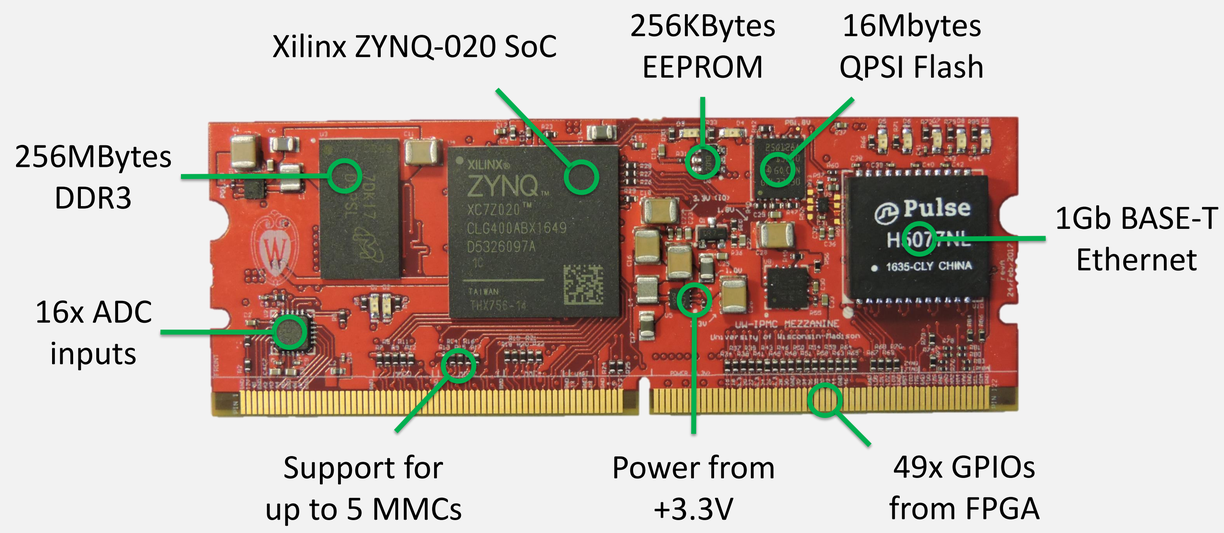
Expandability is provided by the ZYNQ's FPGA section where 73 general purpose input/outputs (GPIOs) and 8 multi-gigabit transceivers (MGTs) are available to the hardware designer and can drive several standards and custom protocols as:

- JTAG Master controller (Xilinx Virtual Cable),
- AXI Chip2Chip (parallel high-speed GPIOs, Aurora),
- PCI Express (x1, x2, x4 and x8 lanes),
- 10Gb Ethernet (XFI, XAIU).

Blade peripherals are connected to GPIOs or MGTs and configured using Xilinx ecosystem, predominantly made up of Xilinx Vivado and standard AXI inter-connectivities. Common peripherals can be other FPGAs (e.g. Xilinx Ultrascape+) or simpler devices such as EEPROMs, allowing them to be accessed and configured through Linux or exposed by Ethernet.

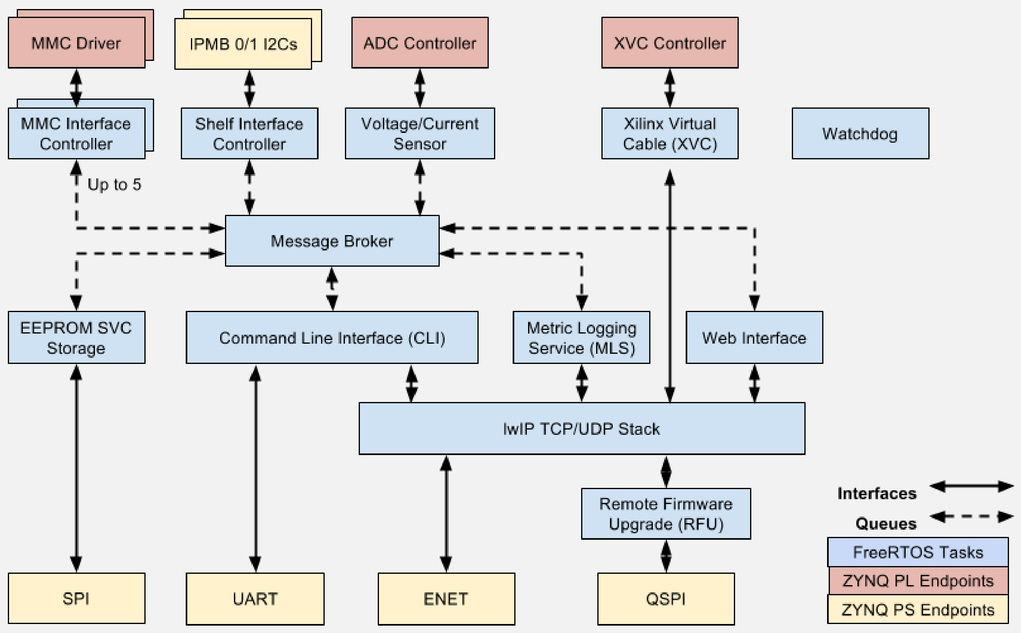


IPMI Controller



The IPMC mezzanine is intended to be the next generation of blade controllers that communicate with ATCA Shelf Managers (ShMC). It is part of the PICMG 3.x specification and each blade needs to have one of such controllers. They are responsible for doing blade related health checks (e.g. temperature, voltages) and to act in case of problems, such as over-temperature or over-voltage.

The IPMC design has a low-cost Xilinx ZYNQ SoC that runs FreeRTOS, which is ideal for time sensitive applications, and uses FPGA logic to do parallel comparisons of sensor data versus threshold values, allowing the IPMC to trigger on alarms at sub-millisecond rates. The firmware uses FreeRTOS queues coupled with a publisher/subscriber broker system to relay important messages across different tasks, allowing easier debugging and logging.



Five independent Modular Management Controller (MMC) interfaces allows the IPMC to manage Advanced Mezzanine Cards (AMCs), this preventing bus locking in case one AMC fails. For expandability, 49 GPIOs are available at the mezzanine connector and wired to the FPGA section, allowing the IPMC to interface with power, monitoring or management related components on the ATCA blade. They can also be used to add more MMC interfaces.

Access to the IPMC is done through Ethernet via the ATCA Hub card or through the IPMI bus.

Module Management Controller

The next generation MMC is provided as a reference design and not as a mezzanine due to its simplicity. The design moves away from RISC architectures to ARM microprocessors by using Atmel's SAM4N. Similarly to IPMCs, several ADCs and GPIOs allow the MMC to manage and monitor AMCs which are pluggable and hot-replaceable modules in ATCA blades. Rear Transition Modules (RTMs) are also supported.

The firmware implementation uses FreeRTOS for time sensitive tasks, such as sensor monitoring and alarming. Communication with the IPMC is done through a dedicated I2C bus.