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Readout Electronics System of the CASCA Front-End Chip for the TPC Based X-Ray Polarimeter

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The CASCA is a 32-channal readout ASIC designed for the TPC based X-ray Polarimeter (XTP). We propose a prototype Readout system of the CASCA chip for the XTP. The system mainly consists of three kinds of modules. The ASIC cards, mounted with CASCA chip, are designed for sampling XTP signals. The Adapter card, edged-mounted with the ASIC card, is in charge of digitizing the output from ASIC card. The Master card provides 8 channels for 8 Adapter cards based Serial-Rapid-IO protocol at 6.25Gbps bandwidth, and transfers data through 10 Gigabit Ethernet, therefore 256 electronics channels are achieved.

Summary

Micro-pattern TPC (Time Project Chamber) based X-ray polarimeter has been demonstrated in recent years for its main advantage of releasing the competition between absorption depth and drift distance. It measures two dimensional photoelectron tracks generated by the incident X-ray photons with one dimensional strip readout. The other dimension is calculated by the drift time from the signal waveform. The polarimeter focuses on the X-ray energy of 2-10 keV whose track length is only several millimeters, and 100 um track resolution, fast sampling rate (˜20MSPS) is required.

The CASCA (Charge amplifier and switched capacitor array) chip designed for XTP is a 32-channal readout front-end ASIC integrated with the front-end part and the SCA (Switched Capacitor Array), the former for amplifying and shaping and the latter for sampling. The sampling rate of the ASIC is designed for 40Msps and the valid readout frequency is 5MHz.

The ASIC card named CASCA_FE is designed for driving the CASCA chip. A high performance differential amplifier is adopted in the CASCA_FE to provide the rail-to-rail output for the ADC (Analog to Digital Converter) in the Adapter card.

The Adapter card named CASCA_AD, edged-mounted with the CASCA_FE, is in charge of digitizing the output from the CASCA_FE. A Xilinx Artix-7 FPGA chip, a 12-bit ADC and a multi-output clock generating chip are mounted on the CASCA_AD. The FPGA chip provides logic signals to make the CASCA_FE working properly, and is responsible for packaging the digital data from the ADC. The ADC provides 10Msps sampling rate and 12-bit accuracy in parallel output, which is able to digitalize the output of the ASIC efficiently. The clock generator is configured to meet the requirement of the sampling clock and readout clock.

The CASCA_AD edged-mounted with CASCA_FE is near to the detector for sampling waveform. And a HDMI cable is adopted to connect the CASCA_AD and the Master card. The initial voltage were supplied via the HDMI cable from Master card, as the same way that the packaged digitalized data, source clock and trigger signal were transferred.

With the help of the Serial Rapid-IO Technology and HDMI2.0 cable, the bandwidth of Dataflow could achieve the maximum of 6.25Gbps. The data transfers through the Serial Rapid-IO protocol realized by the Logic IP Serial Rapid-IO Gen2 Endpoint Solution in the FPGA chip.

The Master card named HPDAQ as a FMC-Based card with two FMC connectors, which is responsible for digital data acquiring and processing, connects to the CASCA_AD through a Mezzanine card. In a way of “Several-in-One”, 8 CASCA_AD cards are connected to one Master card with 8 HDMI cables. And the Master card transmits data to Server over 10 Gigabit Ethernet. A high-performance FPGA and DDR4 are adopted to

provide the logic resource, I/O interfaces and data buffer.
This readout electronics system is flexible to apply in the XTP. One Master card is able to support 256 electronics channels, and a large number of the Master card could be assembled in parallel to meet the requirement of the large XTP.

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