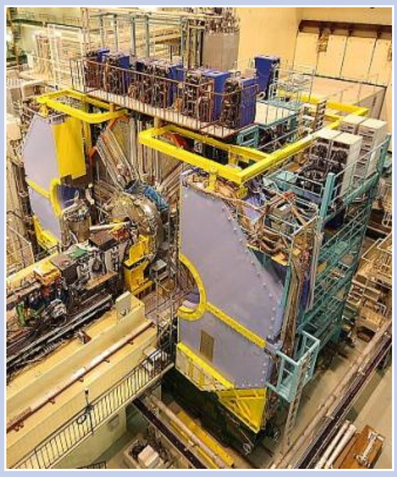
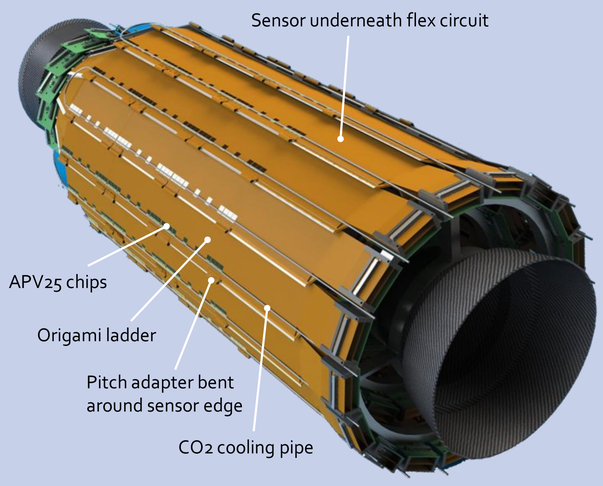
Richard Thalmeier (HEPHY Vienna) for the Belle II SVD Group

Electronics and Firmware of the Belle II Silicon Vertex Detector Readout System

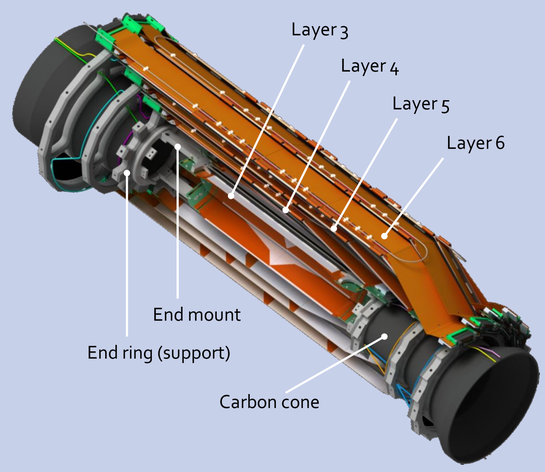
Data flow



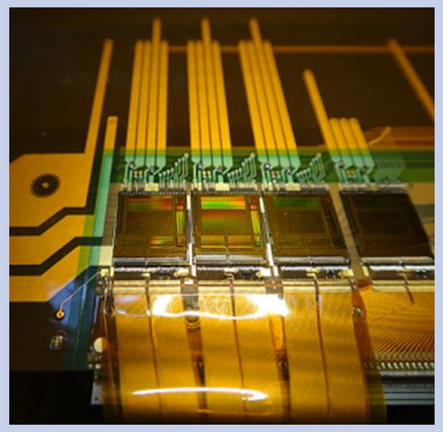
Belle II detector



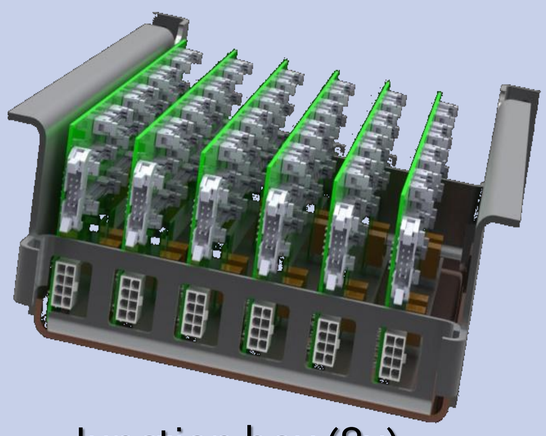
SVD



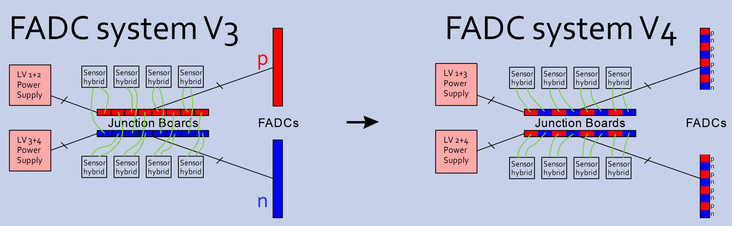
SVD (inside)



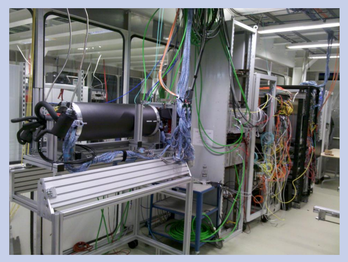
SVD hybrid



Junction box (8x)



Sensor wiring concepts



DESY permanent test setup

Cabling

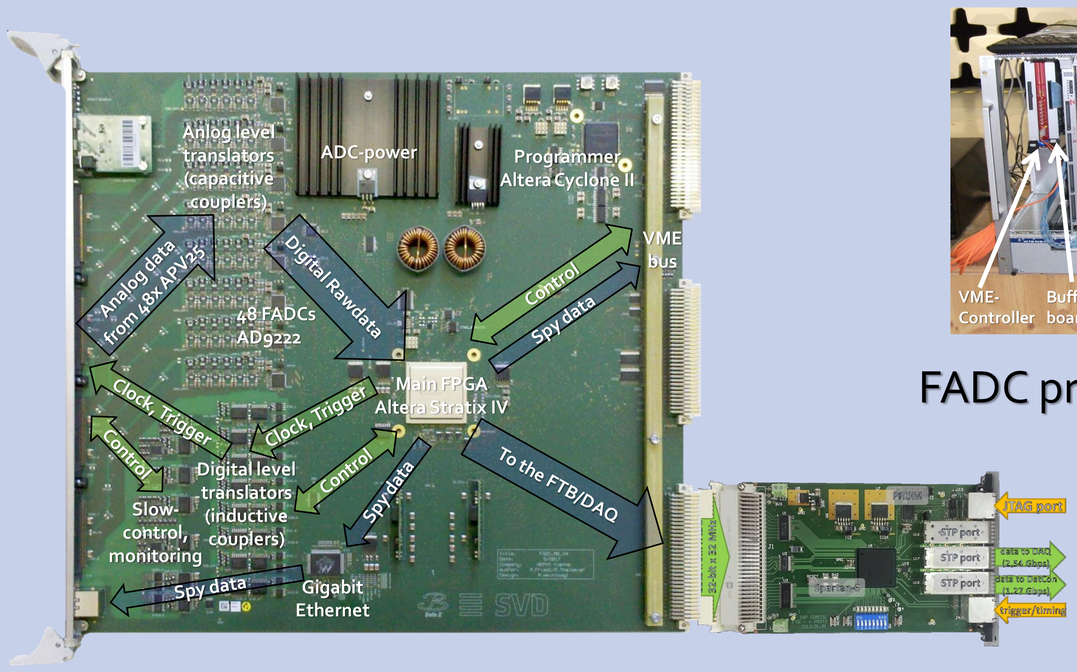
At the High Energy Accelerator Research Organization (KEK) in Tsukuba, Japan, the Belle II experiment will explore the asymmetry between matter and antimatter and search for new physics beyond the standard model.

One of its sensor systems is the Silicon Vertex Detector, which consists of 172 orthogonal double-sided strip sensors arranged cylindrically in four layers around the collision point to measure the tracks of the collision products of electrons and positrons.

These sensors are read out by 1748 radiation-hard CO_2 cooled APV25 front-end chips, which send one time-division multiplexed differential analogue data signal each out of the radiation zone over approximately 15 meter long copper cables to four crates with 48 FADC modules which convert them to digital using one flash analog digital converter per APV25 chip.

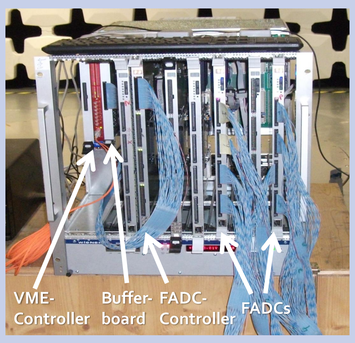
Each of these FADC modules also includes a field programmable gate array chip, namely a Stratix IV GX, which compensates line signal distortions using digital finite impulse response filters and detects data frames in the incoming streams. It reorders the data accordingly to the physical arrangement, performs pedestal subtraction and common mode correction to eliminate static offsets and zero suppression to discard empty strip data, and it calculates the peak timing and amplitude of each event from a set of data samples using a neural network in real-time. Eventually, the processed data are sent to another detector to provide information for timing and the determination of spatial regions of interests, as well as to a data acquisition system which further sends it to a worldwide computer grid for high-level analysis.

The whole SVD readout system has been tested successfully at several test beams (CERN, DESY), as well as in a persistent setup at DESY for more than half a year (2016-12 to 2017-07) with prototypes. Several options in the cabling and hardware have been developed and evaluated to fine-tune the noise robustness and reliability of the SVD system. We now have two candidates for the FADC modules and the corresponding boards in the junction boxes. The main difference is the cabling concept of the power and data lines from the FADC modules to the detector. The decision which version will be used will be made in October 2017 at KEK in Japan, where final noise injection tests will be performed right on the final detector structure. Instantly after this decision, the mass-production of the printed circuit boards will start in Vienna, Austria. The boards will be delivered to KEK in early 2018 and installed in the second half of next year.

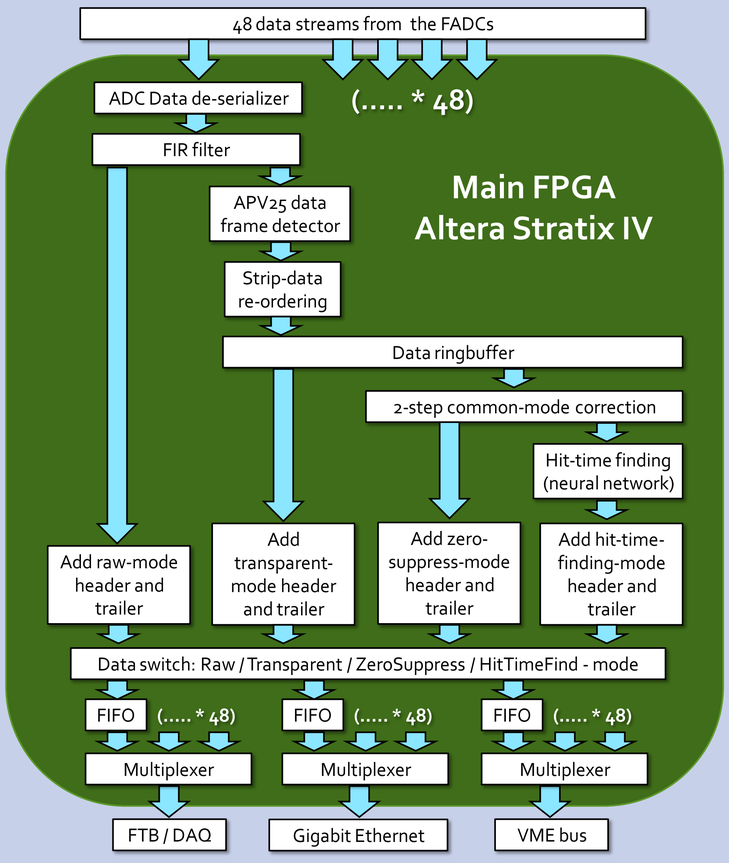


FADC module (48x)

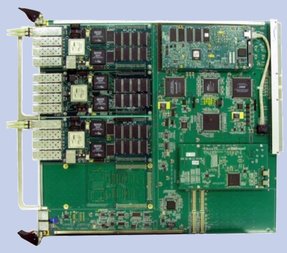
FTB (48x)



FADC prototype crate



FADC firmware (Data path)



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