Contribution ID: **116** Type: **Poster**

Electronics and Firmware of the Belle II Silicon Vertex Detector Readout System

Wednesday 13 September 2017 17:45 (15 minutes)

The Silicon Vertex Detector of the Belle II Experiment at the KEK in Tsukuba, Japan, consists of 172 double-sided strip sensors. They are read out by 1748 APV25 chips, and the analogue data are sent out of the radiation zone to 48 modules which convert them to digital. FPGAs then compensate line signal distortions using digital finite impulse response filters and detect data frames from the incoming stream. Then they perform pedestal subtraction, common mode correction and zero suppression, and calculate the peak timing and amplitude of each event from a set of data samples using a neural network.

Summary

At the High Energy Accelerator Research Organization (KEK) in Tsukuba, Japan, the Belle II experiment will start in 2019 to refine the exploration of the asymmetry between matter and antimatter of the original Belle experiment with a 40 times higher luminosity of 8x10^35 cm-2s-1, and to search for new physics beyond the standard model by measuring the tracks of the collision products of electrons and positrons. This requires a redesign of the detector and its peripherals.

One of the Belle II sensor subsystems is the Silicon Vertex Detector, which consists of 172 orthogonal double-sided strip silicon sensors made of 6 inch wavers each. They are arranged cylindrically in four layers around the collision point. These sensors are read out by 1748 radiation-hard CO2 cooled APV25 front-end chips, partially sitting directly on the sensors (”Origami” chip-on-censor-concept), and powered by radiation-hard DC-DC converters in junction boxes inside the magnetic field. One time-division multiplexed differential analogue data signal is sent by each one of these read-out chips out of the radiation zone over approximately 15 meter long copper cables to four crates with 48 so called FADC modules, which convert the data streams to digital using one flash analog digital converter per APV25 chip.

Each of these FADC modules also includes a field programmable gate array (FPGA) chip, namely an Altera Stratix IV GX, which compensates analog line signal distortions using digital finite impulse response filters, and detects data frames in the incoming streams. It then reorders the strip signal data according to the physical arrangement, performs pedestal subtraction and common mode correction to each strip value to eliminate static offsets, executes zero suppression to discard empty strip data for data size reduction, and it calculates the peak timing and amplitude of each event from a set of data samples using a neural network in real-time to further reduce the amount of data. Eventually, the processed data are sent to the pixel detector to provide information for timing and the determination of spatial regions of interests, as well as to a data acquisition system which collects the data of all subdetectors and performs high level trigger data selection.

We will show an overview of the Silicon Vertex Detector data readout system, from the detector itself with its front-end electronics, over the cabling, junction boxes, power supplies for the read-out chips and the “high voltage” biasing of the silicon sensors, read-out-signal potential separation and digitization, to the data processing inside the FPGAs on the FADC modules and the data output systems. Furthermore we will present most recent test results of the prototypes of the system in beam tests and long-term-tests, improvements we applied to the electronics with comparisons to previous prototypes, and first analysis results of simulations of the expected performance of the neural network for the hit time finding system in the FADC firmware.

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Session Classification: POSTER Session

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience