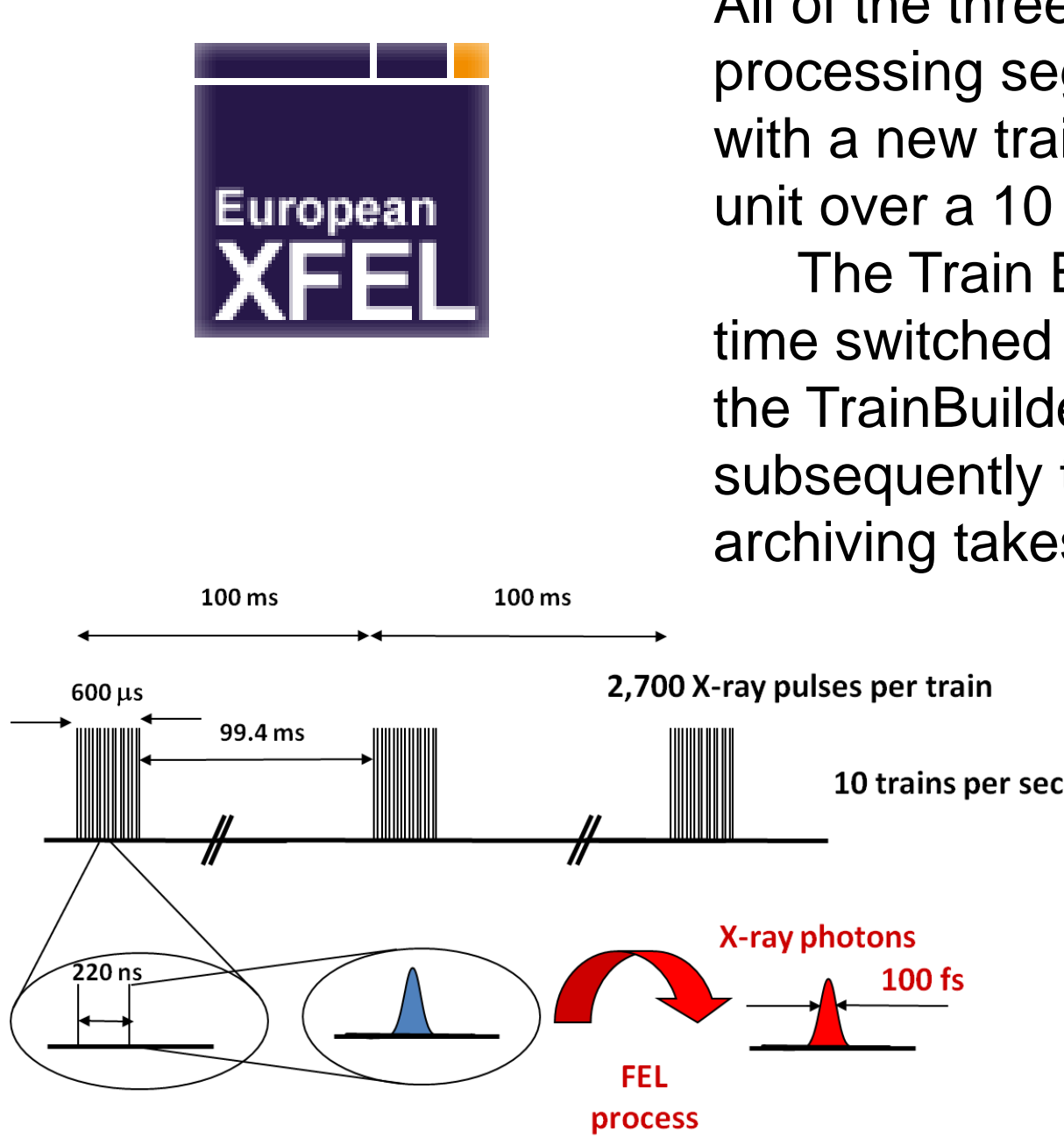
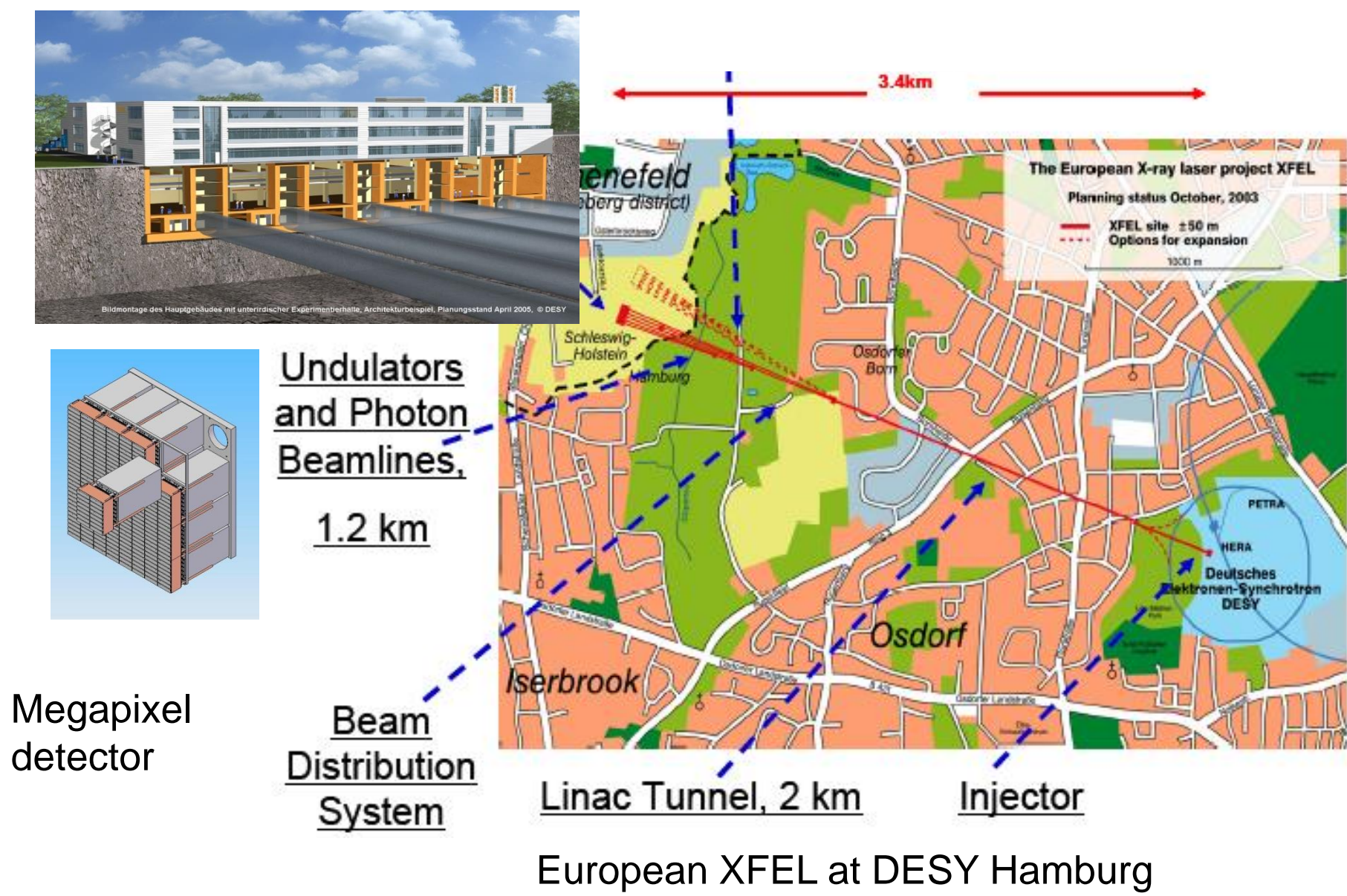


The Train Builder Data Acquisition System for the European-XFEL

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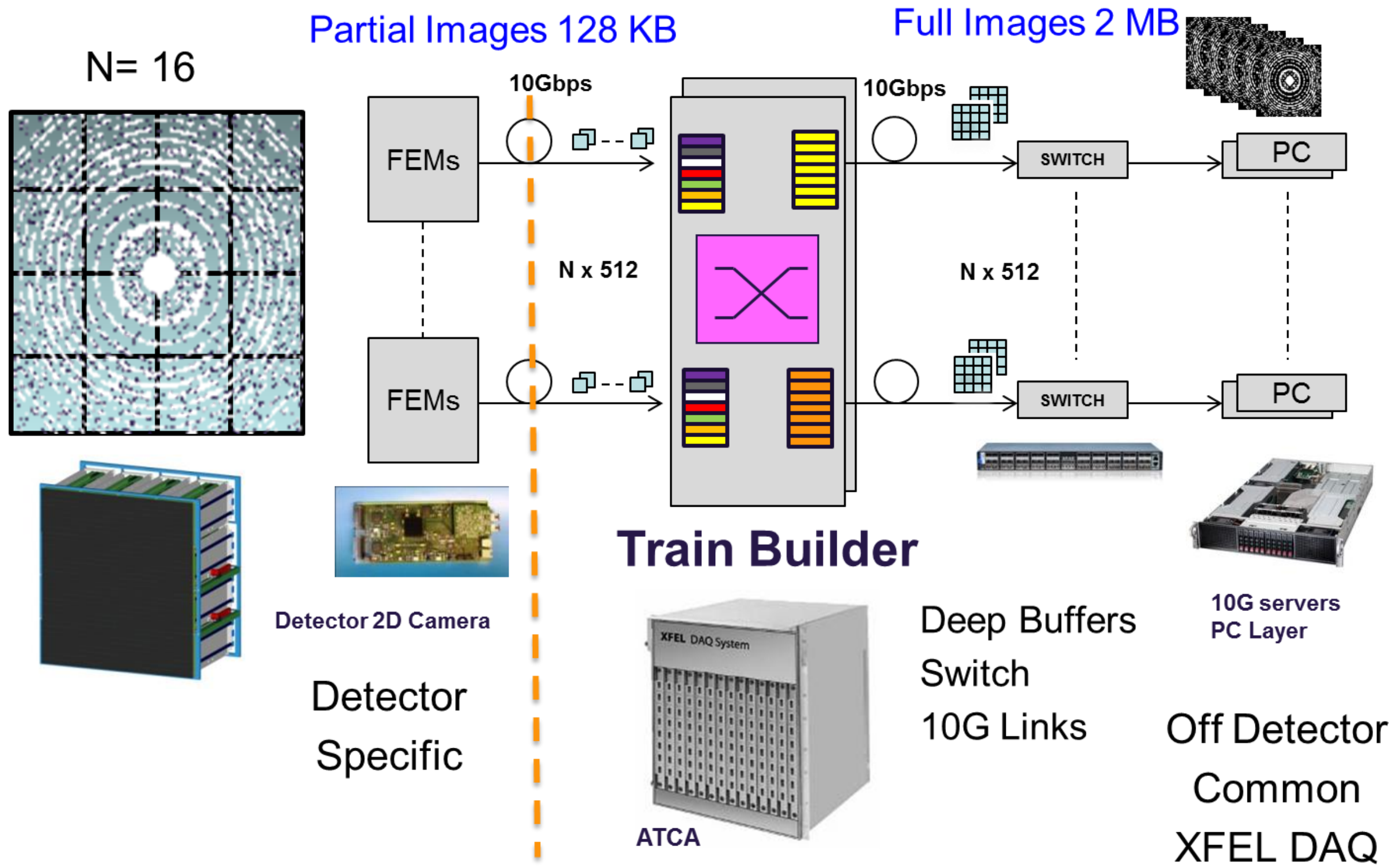
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XFEL Data Acquisition

All of the three 2D Megapixel detector designs are modular with integrated Front End Electronic (FEE) units processing segments of the pixel array. Images from up to 510 X-ray pulses are captured during each train with a new train arriving every 100 msec. During the long 99 msec inter-train gap data is sent from each FEE unit over a 10 Gbps optical link using UDP/IP protocol to the TrainBuilder.

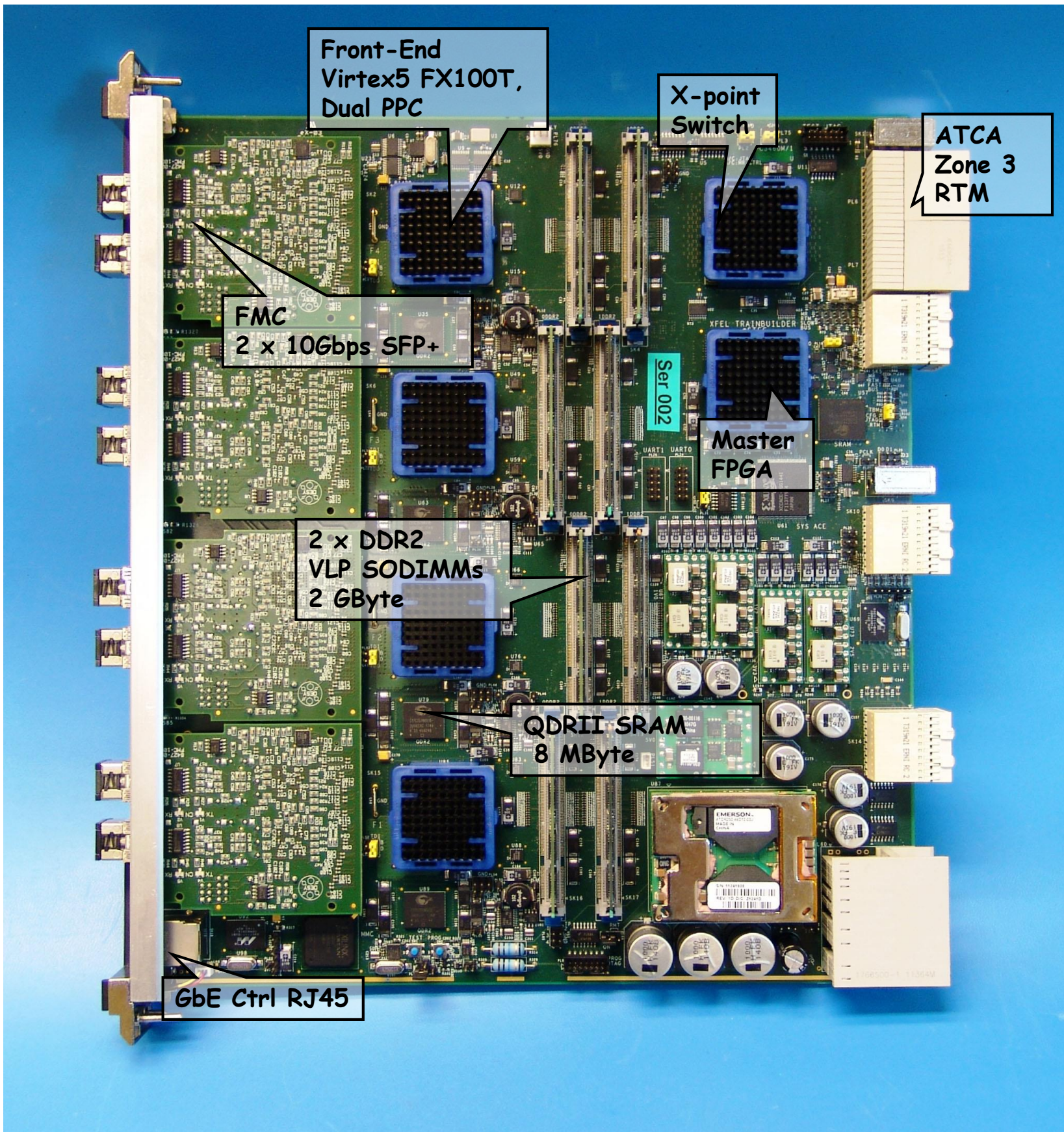
The Train Builder exploits the regular time structure of the data flow from the XFEL detectors and uses a time switched multiplexing architecture to assemble complete series of images from entire trains. In addition the TrainBuilder carries out initial image processing and data formatting. The resultant train "movies" are subsequently transmitted over another set of 10 Gbps links to a farm of PCs where final image processing and archiving takes place.



Introduction

The European XFEL will generate ultrashort X-ray flashes with a brilliance that is a billion times higher than that of the best conventional X-ray radiation sources. Starting in autumn 2017, it will open up completely new research opportunities for scientists and industrial users. The XFEL beam timing and detector data rates are comparable to those found in particle physics facilities.

The beam lines will be instrumented with three different designs of Megapixel 2D planar silicon detectors. STFC Technology is designing a common off-detector data acquisition system for all these detectors (TrainBuilder) using the AdvancedTCA specification.



TrainBuilder I/O board

TrainBuilder ATCA I/O Board

- 4 x Input/Output channels each comprising of :
- VITA57 FMC slot housing dual 10 Gbps SFP+ optical transceivers with 10 G XAUI interface.
 - Xilinx Virtex5 (FX100T) FPGAs. 16 Multi-Gigabit Transceivers. Dual PowerPC processor embedded memory controllers with DMA offload engines.
 - Dual DDR2 VLP SODIMMs (each up to 2 GByte). Each channel can be programmed to be a 10GbE Input from a FEE link or an Output to a PC link.
 - QDR II (8 MByte) for image processing.

Backend comprising of:

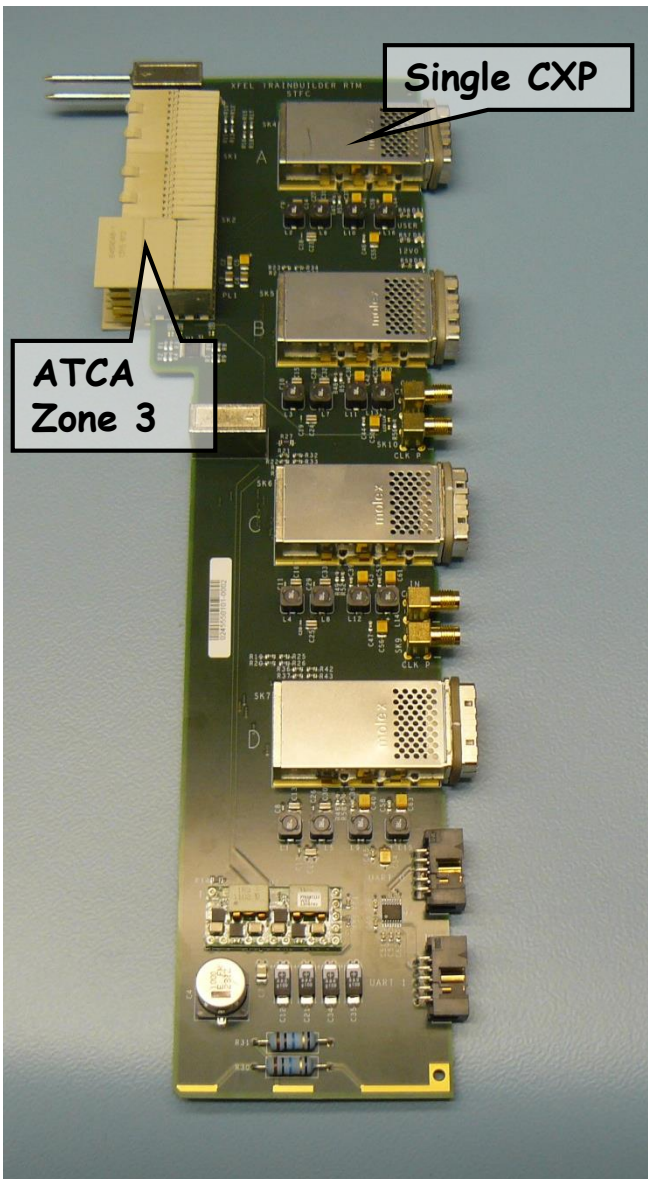
Analogue Crosspoint switch (Mindspeed M21145) (72x72 lanes)

ATCA Zone 3 with 32 Tx & Rx Multi-Gigabit lanes.

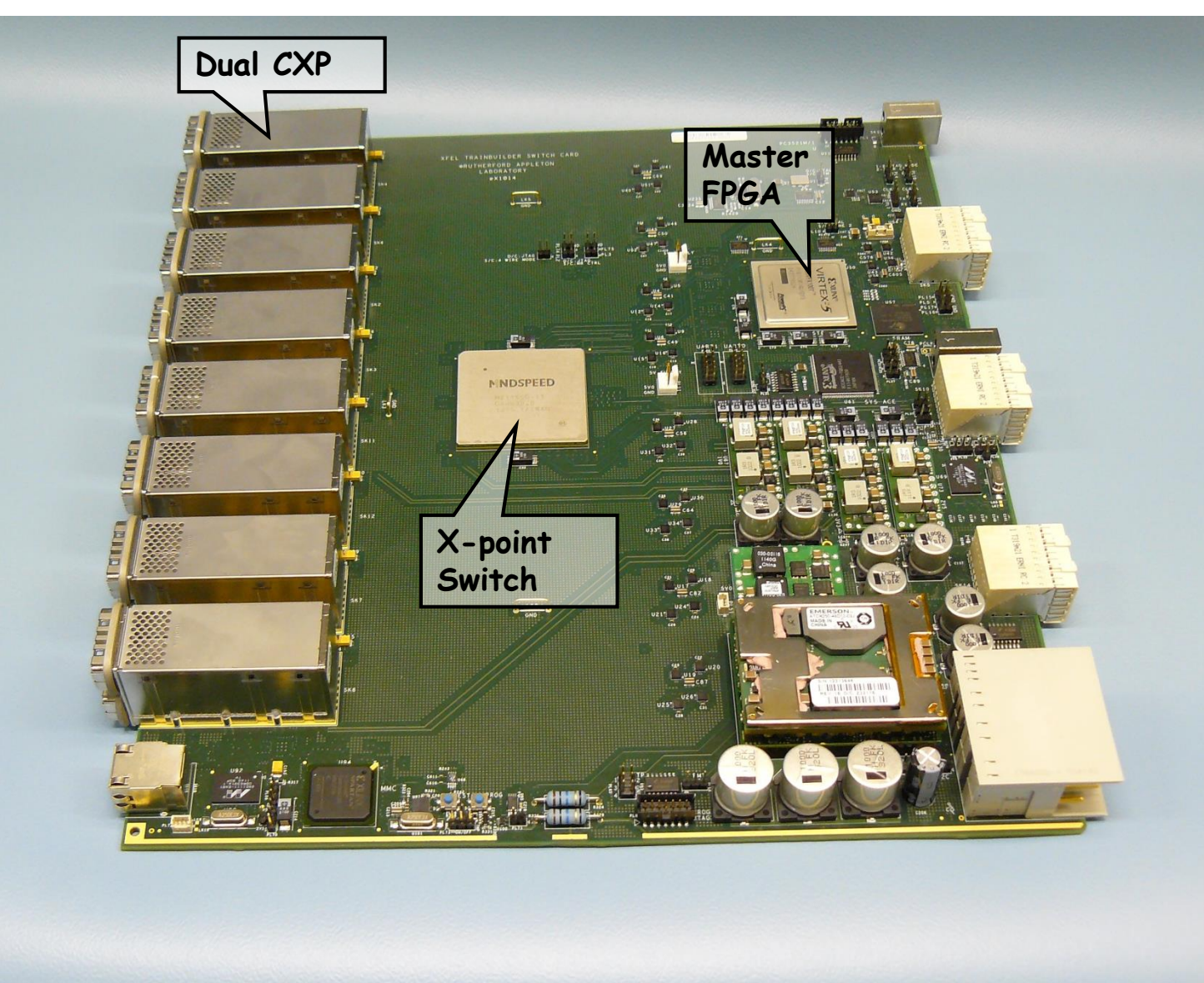
Master Virtex 5 FPGA for switch synchronisation.

Module Management Unit (MMC) Spartan3 FPGA with embedded Flash.

GbE interfaces on Front panel and via ATCA Zone 2 for control and monitoring.



Rear Transition Module



TrainBuilder Switch board

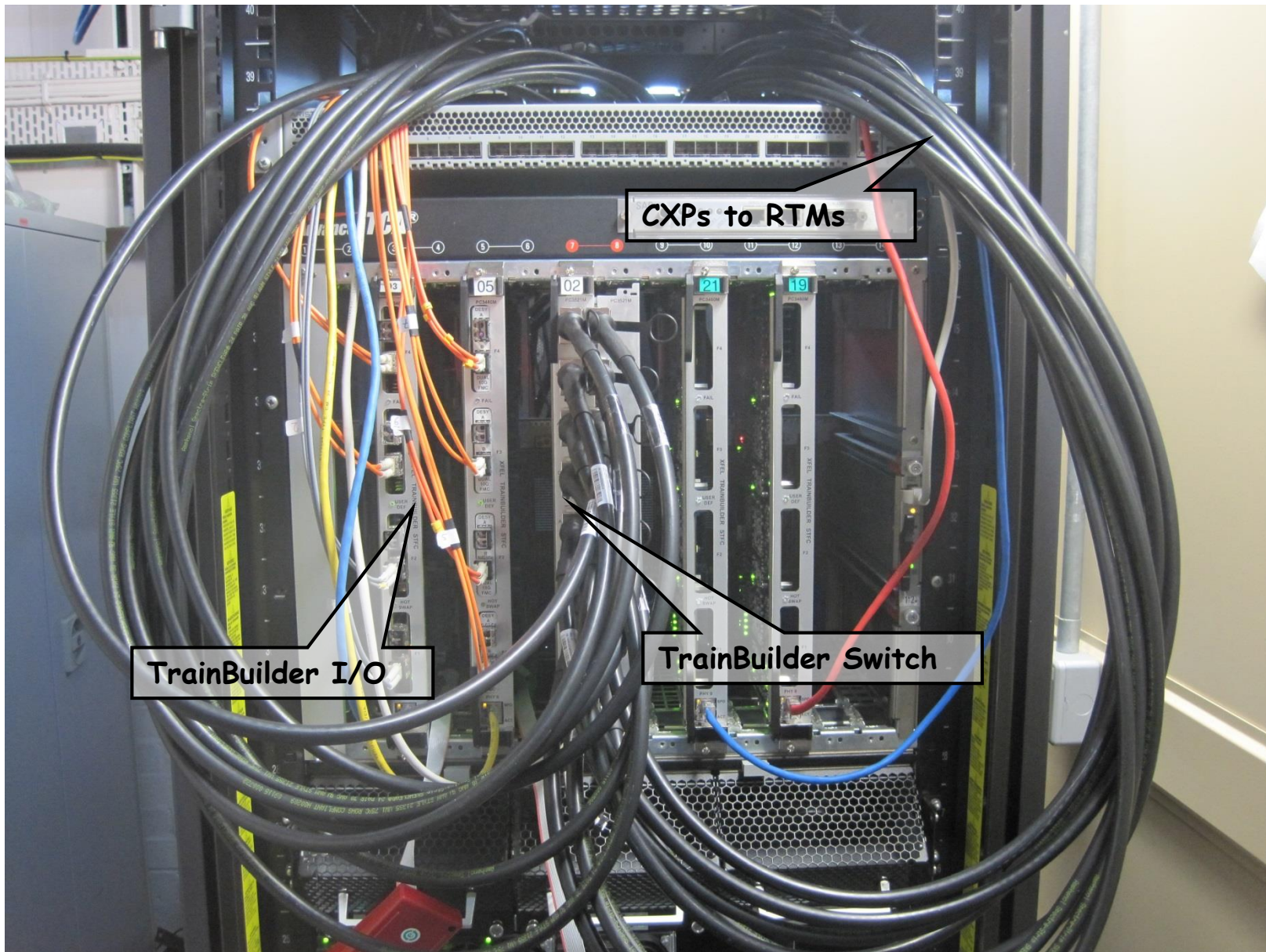
Megapixel System boards

A single TrainBuilder I/O is sufficient to instrument prototype 1/4 Megapixel (Quadrant) detectors.

For full megapixel detectors four TrainBuilder I/O boards are used together with a dedicated Switch board.

The boards are interfaced with ATCA Rear Transition Modules (RTM). Data and controls are transmitted on CXP standard cables (either copper or optical) using the Xilinx Aurora protocol.

The main purpose of the Train Builder is to feed each Farm PC with complete images from all the X-ray pulses captured during any given train. The crosspoint switch is operating as a time multiplexed barrel shifter.



TrainBuilder ATCA Crate

FPGA Firmware

The FPGA I/O design consists of Detector Input and Output processing modules:

- 2 x 10G block with 10 GbE UDP/IP protocol engines interfaced to the Xilinx XAUI core. Distributes train outputs to PC Farm according to data Train ID. Optimised for UDP Rx from FEE links and Tx to PC links.
- Deep data buffering for complete Trains (1 GB per Train). Dual Power PC DDR2 memory controllers each using multiple DMA offload engines for concurrent memory Read & Write.
- Image Processing module interfaced to QDR II SRAM.
- XFEL event data formatting.
- Aurora serial protocol block for data Tx and Rx across the switch, employing 8B/10B encoding.

All blocks are interconnected using the Xilinx LocalLink synchronous stream protocol with arbitrary frame lengths.

Status

Four TrainBuilder ATCA crate systems are currently being commissioned with detectors and the PC Farm at XFEL. Two of the three Megapixel detectors (LPD and AGIPD) are expected to be ready for first X-ray beams in Autumn 2017. The first experiment data taking with the TrainBuilder included in the readout chain is planned for November 2017.