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Design of the New Front-End Electronics for the Readout of the Upgraded CMS Electromagnetic Calorimeter for the HL-LHC

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At the high-luminosity upgrade of the LHC (HL-LHC), the electromagnetic calorimeter of CMS (ECAL) will have to cope with a challenging increase in the number of interactions per bunch crossing and radiation levels. The ECAL front-end readout electronics was completely redesigned, with the goals of providing precision timing, low noise and added flexibility in the trigger system. It will use a faster pre-amplifier, increase the sampling frequency from 40 MHz to 160 MHz and implement a trigger system that resides entirely off-detector. The design of this new electronics will be presented along with the test results of the first prototypes.

Summary

The electromagnetic calorimeter (ECAL) of CMS is currently operating at the LHC. The instantaneous luminosity during the current LHC Run2 is in the range of up to 2×10^{34} cm^{-2}s^{-1} in routine operation. With an upgrade at the end of the decade, the High-Luminosity LHC (HL-LHC) will increase the instantaneous luminosity by about a factor of 2 to 5 from current levels. The goal of the HL-LHC is to accumulate a total of at least 3 ab-1 of data.

With such high luminosity and consequent event rate, the primary driver of the ECAL front-end electronic upgrade are the requirements on the first level of the CMS trigger system, implemented with custom-design hardware boards. Specifically, the latency has to be of 12.5 μs, about a factor of two more than the current electronics, and the sustainable rate must go up to 750 kHz, about a factor of five more than the current design.

The front-end readout electronics was completely re-designed to satisfy these requirements, and the opportunity was taken to optimize the mitigation of radiation-induced noise increase in the APDs, the rejection of APD anomalous signals, and the time resolution of the arrival of electromagnetic showers.

The individual boards of the new electronics will follow the same configuration and form factor as the present ones, mostly imposed by the decision not to modify the cooling system or the motherboards connecting the very-front-end (VFE) to the crystal APDs. The VFE pre-amplifier will reduce as much as possible the shaping time of the signal, by employing a Trans-Impedance Amplifier (TIA), which will sample the pulse at 160 MHz. Two gain stages will follow and digitize signals up to 2 TeV with 2 12-bit ADCs. High-speed optical links and their foreseen evolutions at 10 Gb/s (lp-GBT) will enable us to send to the off-detector electronics all the single crystal data via a data transmission unit with lossless compression.

The system will use 130 nm CMOS technology for the replacement of analogue ASICs and 65 nm technology for digital ones, which are both naturally radiation-tolerant and provides up to 75\% gain in power consumption. A specific low-voltage regulator card is being developed to provide all the required bias voltages. Control signals and clock distribution will be provided by (redundant) GBTX control buses.

The talk will discuss in detail the requirements of the new ECAL front-end electronics along with the design options and adopted choices to fulfill them. It will also show the results of beam tests performed with a first prototype of the TIA electronics using discrete components.

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